DEWAR ELECTRONICS

[redacted]

DM1200 Series Teleprotection

Technical Description

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Technical Description.

1. Introduction.

The use of the leading edge technology has resulted in the DM1200 being of simple construction with minimum component count, leading to enhanced reliability. Through a menu driven LCD and software control the user has full set up, control and supervision over the system parameters without resort to extender boards, trimpot adjustments or add on instruments such as PC's, programmers or compilers. Set up can also be achieved directly or indirectly (by setup upload) through a modem or PC over RS232 if needed.

The DEWAR DM1200 series teleprotection system allows for blocking, permissive, direct tripping and many other applications. It has the latest in innovation and technology, to meet the demanding reliability, security and dependability requirements of electric power authorities world-wide.

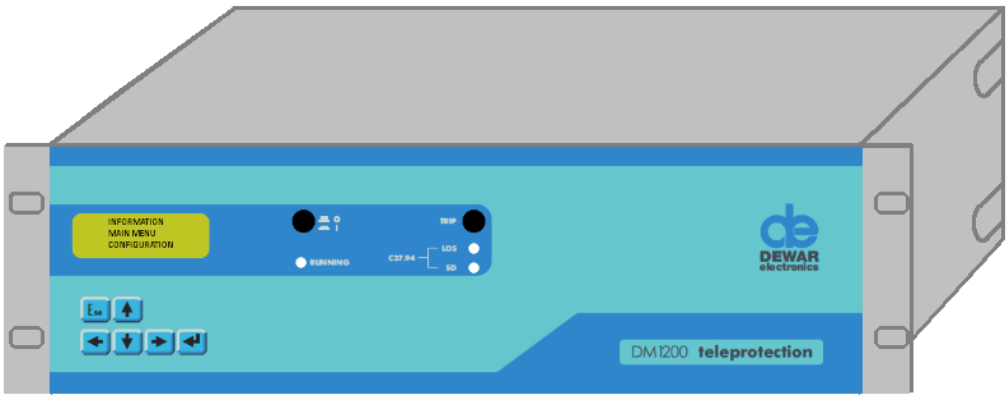


Figure 1a Model DM1200 Terminal Front.

1.2 DM1200 G703 Terminal.

- 3U by 19 inch subrack enclosure, with termination board,
- Power Supply card, 20 to 60VDC or 90 to 320VDC,
- Monitor Module (LCD display with soft-touch switches and software control),
- Up to four trip I/O modules. Rated output at 2amp @ 240VDC,
- G703 Processor module, for CCITT G703 64 kilobaud through digital bearers,
- Optionally 1 or 2 Alarm Relay cards (8 by 1C/O relays per card).

1.3 DM1200 RS422 Terminal.

- 3U by 19 inch subrack enclosure, with termination board,
- Power Supply card, 20 to 60VDC or 90 to 320VDC,
- Monitor Module (LCD display with soft-touch switches and software control),
- Up to four trip I/O modules. Rated output at 2amp @ 240VDC,
- RS422 Processor module, 9KBaud to 80Kbaud, electrically compatible with RS530, RS449 and other standards,
- Optionally 1 or 2 Alarm Relay cards (8 by 1C/O relays per card).

1.4 DM1200 VF Terminal.

- 3U by 19 inch subrack enclosure, with termination board,
- Power Supply card, 20 to 60VDC or 90 to 320VDC,
- Monitor Module (LCD display with soft-touch switches and software control),
- Up to two trip I/O modules. Rated output at 2amp @ 240VDC,
- VF Processor module,
- High speed "Loss of Guard" capability,
- Optionally 1 or 2 Alarm Relay cards (8 by 1C/O relays per card).

1.5 DM1200 C37.94 Terminal.

- 3U by 19 inch subrack enclosure, with termination board,
- Power Supply card, 20 to 60VDC or 90 to 320VDC,
- Monitor Module (LCD display with soft-touch switches and software control),
- Up to four trip I/O modules. Rated output at 2amp @ 240VDC,
- C37.94 Processor module, for IEEE C37.94 N times 64 kilobaud through optical bearers,
- Optical communication module with 850nm multi-mode for 2km and 1310nm multi-mode for 2km and 1310nm single-mode for 20km,
- Optionally 1 or 2 Alarm Relay cards (8 by 1C/O relays per card).

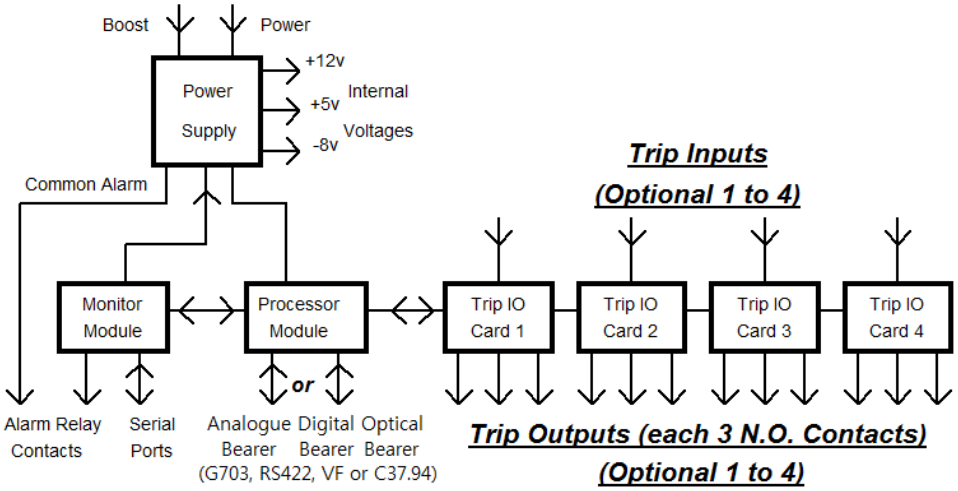


Figure 1b Terminal Modules and Cards

2. DM1200 Features.

- Firmware control. Large number of default setup tables. Setup self checking. Performance checking.
- Dual microprocessor architecture.
- All major system parameters under user control.
- Automatic self test (8 times per second, includes the trip input and trip out wiring) and Manual test.
- Self diagnostics to component level
- 80 character LCD display provides full setup and monitoring facilities.
- No internal or front panel trimpots adjustments. No add on requirements for programming.
- Serial ports for remote logging.
- Selectable user passcode entry to setup, maintenance and manual test menus.
- End to end supervisory channel.
- User programmable security and dependability, independent for each trip IO card, to suit user application.
- Hardware and software dual complimentary paths ensures that no single component failure can cause a trip.
- Time stamping of events. History of previous events down load capability.
- Communcation error monitoring as per ITU-T G.821 standard.
- User programmability via soft-touch switches. Setup and testing is menu driven. Software displays information on the LCD display. An RS232 / RS485LAN testing and setup available via a PC or modem connection.
- CCITT G703 64KBaud communications; co-directional or contra-directional digital link, 500VDC isolated.
- RS422 (V11) 9KBaud to 80Kbaud communications; slave or master clocking for direct or digital link, 1000VDC isolated.
- Extended CCITT G232 voice frequency coomunications on an analogue link, 5000VDC isolated.
- IEEE C37.94 N (N = 1 to 12) times 64KBaud communication; internal or recovered clock. Support optical multiplexing and secure communication over 2km or 20km distances on multi-mode or single-mode fibre respectively.
- The G703, RS422 and C37.94 processor modules can operate 1, 2, 3 or 4 trip IO cards giving 1 to 4 independent trip command functions.
- The C37.94 processor module provides simple UI for signal error indicators and optical module ID display.
- The VF processor module has two VF transceiver channels. These can be configured in three variations.
  1.As a dual channel high security command system requiring 1 trip IO card.
  2.As a single channel system requiring 1 trip IO card.
  3.As 2 single channel systems requiring 2 trip IO cards.
- VF Loss of Guard capability. For interface to trip breaker logic.
- Alarms can be logically "ORed" to any relay and a pair of relays can be programmed to operate as a dual changeover. The alarm relays are provided in groups of 8. For 16 alarm relays, two relays cards are required. Also a common alarm relay, on the power supply card, can be programmed to operate with any alarm combination.
- Non-volatile EEPROM setup storage. Duplicated write operations are stopped to extend EEPROM life.
- Battery back up memory and time clocks
- Supervisory link allows remote terminal identification, time locking, testing, etc.
- Modular construction:- 1, 2, 3, or 4 trip commands as required
- Three separate trip input voltages 240VDC, 120VDC and a LOW voltage range. The LOW voltage can set to 24, 32 or 48VDC with a jumper setting on the trip IO card.
- Trip output range, 2amp 320VDC maximum.
- Each trip I/O has three programmable "normally open" or “normally close” output contacts.
- Two power supply ranges are available, 20 to 60VDC and 90 to 320VDC (ordering option).
- DM1200 systems are housed in a standard 3U by 19 inch subrack. As all DM1200 systems use the same subrack and support modules, changing communications is achieved by simply changing of the processor module.
- Isolation and HFD to IEC834-1 and IEC255 standards
- Performance testing to IEC60834-1.
- Remote access to set up, status, history of events

3. Command Processing and Security

Trip processing is achieved by dual complimentary paths. Each trip signal has a guard signal of opposite in polarity. This complimentary philosophy extends to trip processing elements (e.g. timers, communications bits, etc.). A timer used for a trip has a complimentary guard timer. To allow a trip output to happen the trip must be a "1" and the guard a "0". This forms part of the basic teleprotection specification of "no single component failure may cause a trip". Under normal operation, any section of the processing, where the trip and guard are not complimentary, a guard condition is output from the processing section (eg a trip extend timer).

The security of a system against the generation of false trips as a result of communication faults, noise or crosstalk, is a trade-off against speed of operation and dependability.

To guard against false trips, the DM1200 has dual complimentary signal. These dual trip paths commence immediately after the trip input dropping resistors and continue right through to the trip output terminals. These paths incorporate opto-isolators, microprocessor I/O ports, software functions and memory locations, communication code words and design specific solid state output switches. The components used for the two paths do not share common packages and signal levels are complimentary. A trip must be registered in both paths for a trip to be validated.

Such redundancy is of limited value unless component failure can be detected. For this purpose the DM1200 self test routines provide continuous automatic detection of failed components.

There are other sources of poor security that are often given insufficient consideration. One of these is the trip input circuit where unwanted signals can be induced. The DM1200 teleprotection systems have a threshold of current which must exceed a minimum level for a user adjustable ‘debounce' time (to suppress spikes), before a trip is accepted.

3.1 G703, RS422 and C37.94 Security

With digital and optical communication, the response time is short so that only the security / dependability trade-off needs be to considered. The security is set by specifying the number of uncorrupted words that must be received within a nominated window. The use of error detecting line codes and sequential frame numbering enables the detection of data which has been corrupted by abnormalities such as bit errors, jitter, foreign signal sources and noise. As an option, terminals may be ‘paired' to protect against the possibility of crossed communication channels.

3.2 VF Security

With voice frequency (VF) communication, the response can be long so that security / dependability / response time trade-offs need be to considered. Each VF receiver channel has two independent and conceptually different detectors. Each receiver channel detects noise, trip or guard conditions. The security is set by qualifying timers, noise inhibit timers and also by setting the thresholds of the receiver detectors.

3.3 Inbuilt Setup Aids

The DM1200 has a number default setup tables covering all communication modes in most application requirements. The default tables are built into the terminals firmware. In addition to these tables, the DM1200 allowes the user to specify a performance (or application) setting to allow the user to easily change individual settings and maintain the required performance.

4. G703, RS422 and C37.94 Processing.

Transmit data, receive data and clocks are electrical isolated. The data stream processing is implemented in an EPLDs for digital processor cards and in a FPGA for optical processor card. A digital signal processor (DSP) encodes and decodes the trip, guard, line checking codes and supervisory data in a framed data packet.

4.1 G703, RS422 and C37.94 Data Packets.

The data transmitted on the bearer is 4 or 5 octets, depending on users settings. In all packets there is 16 check bits and 16 data bits. The data bits contain octet marker bits, supervisory data, four trip bits, four guard bits, and sequence bits. The octet marker bits provide identification of which octet has been received.

- supervisory data bit is a low speed asynchronous serial channel. Due to the low speed and special software, it can still operate with high bit error rates.
- four trip bits mirror the state of the trip inputs.
- four guard bits mirror the state of the guard inputs. Due to the dual complimentary processing philosophy the guards bits will be opposite polarity to the trip bits.
- sequence bits provide a packet signature check. This stops systematic errors from the multiplexers causing false trip operation. Each transmitted packet is encoded with a number in a predetermined manner. As each packet is received its sequence number must match with an expected sequence number. Because the sequence changes with each packet, the 16 check bits and 16 data bits are continually changing, so any statistically imposed bit pattern from a failing multiplexer cannot cause trip operation.
- check bits are distributed through each octet in such a way that any octet having errors can be identified.

4.2 G703, RS422 and C37.94 Trip Input Processing.

Refer figure 4.2.

- "trip input interface" provides the electrical path to the DSP. The electrical trip input drives dual optocouplers, initiating the trip / guard philosophy.
- "debounce timers" removes contact bounce from trip (or guard) input signals. The timers are implemented by the DSP. The amount of debounce time is controlled by user setup in the monitor module.
- 'input extend timers" allow the duration of trip (or guard) transmission to be extended to allow short trip transmissions to have enough time to operate. The timers are implemented by the DSP. The amount of extension time is controlled by user setup in the monitor.
- "trip sent counters" increment each time the trip is a one level and guard is a zero level. The counters are implemented by the DSP, output to monitor module for display and storage.
- "digital encoder" combinations the trip and guard signals into the data packet for transmission.

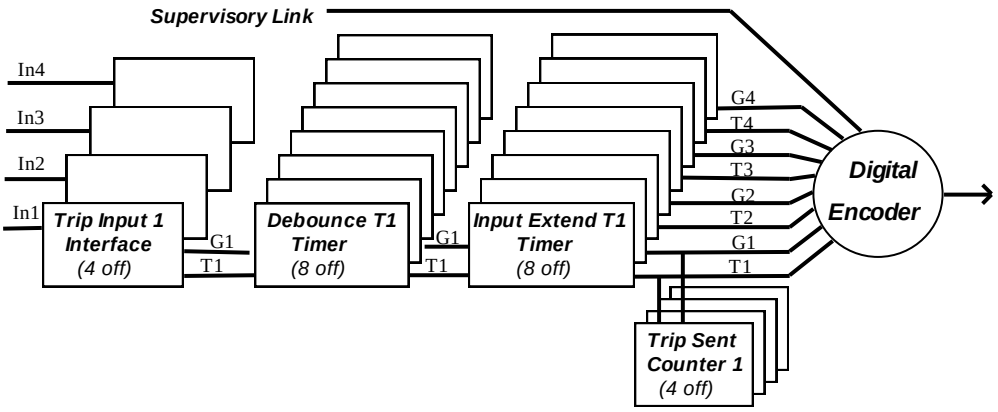


Figure 4.2 G703, RS422 and C37.94 Input Processing

4.3 G703, RS422 and C37.94 Trip Output Processing.

Refer figure 4.3

- "digital decoder" extracts the trip, guard, supervisory data and bit errors from the data stream input. During “SIGNAL LOST” or “AIS” conditions the decoder applies the default output conditions as per the users setup, being “FORCE to GUARD”, “FORCE to TRIP” or “MAINTAIN OUTPUT”. The decoder is implemented by the DSP.
- "bit error count" accumulates total bit errors. The DSP calculates the bit error rate (BER) in parts per million (PPM). The BER is sent to the monitor module for alarm activation.
- trip output security is controlled by a function block including the "‘M' shift register", an add/subtract ‘NM' controller, "‘N' counter" and a "comparator". The ‘M' shift register is ‘M' bits long. As valid trip (or guard) levels are received, they are shifted into the register and increment the ‘N' counter by one. As each valid trip (or guard) is shifted out of the register, the ‘N' is decremented by one. In this way the number of valid trip (or guard) signals accumulated. When the value in the ‘N' counter is equal to or greater than ‘N', a valid trip (or guard) signal is output to the "hold off timer". The values of ‘N' and ‘M' are setup by the user. Maximum security is ‘N'=16 and ‘M'=16, typical values are ‘N'=4 and ‘M'=8. The setting for ‘N’ and ‘M’ for each trip command is independently set by the user. Security is implemented by the DSP.
- "hold off timer" stops multiple trips close together from output before equipment connected to the "trip output interface" has had time to reset. The amount of hold off is setup by the user. The "hold off timer" is implemented by the DSP.
- "output extend timer" allows the duration of trip (or guard) transmission to be extended to allow short trip receptions to have enough time to operate. The timers are implemented by the DSP. The amount of extension time is controlled by user setup in the monitor.
- the "termination timer" can be set to remove trip (or guard) signals after a time-out period set by the user. The "termination timer is implemented by the DSP.
- "trip received counters" increment each time the trip is a one level and guard is a zero level. The counters are implemented by the DSP, output to monitor module for display and storage.
- "trip output interface" combines the trip and guard signals. The output contacts close when the trip is a one level and the guard is a zero level.

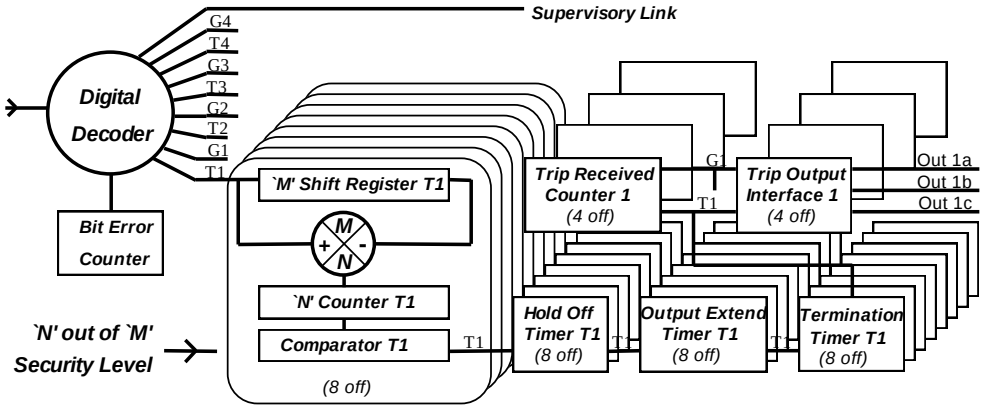


Figure 4.3 G703 and RS422 Trip Output Processing

5. VF Processing.

The VF processor contains two independent FSK transmitters and two independent FSK receivers. The VF transmitters and receiver use microprocessor controlled switched capacitance filters and EPLD based frequency generation. The frequency generators for the transmitters and receivers are derived from a quartz crystal.

The channel frequency can be set to any frequency from 300 hertz to 4095 hertz in 1 hertz steps. The FSK shift can be set from 20 hertz to 500 hertz in one hertz steps. The wide range of frequecnies and shifts allowes multiple DM1200 VF terminals to share a common 4 kilohertz analogue channel.

The receiver detectors and command processing is done by firmware.

5.1 VF Trip Input Processing

Refer figure 5.1

- "trip input interface" provides the electrical path to the microprocessor (uP). The electrical trip input drives dual optocouplers, initiating the trip / guard philosophy.
- "debounce timers" removes contact bounce from trip (or guard) input signals. The timers are implemented by the uP. The amount of debounce time is controlled by user setup from 0 to 99mS.
- 'input extend timers" allow the duration of trip (or guard) transmission to be extended to allow short trip transmissions to have enough time to operate. The timers are implemented by the uP. The amount of extension time is controlled by user setup from 0 to 990mS.
- "trip sent counters" increment each time the trip is a one level and guard is a zero level. The counters are implemented by the uP, output to monitor module for display and storage.
- "VF state encoder" controls the transmission state of each VF channel.. The encoder is implemented by the uP.

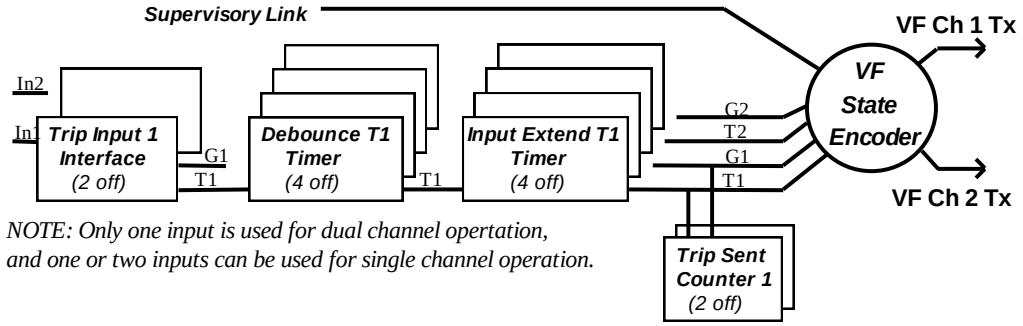
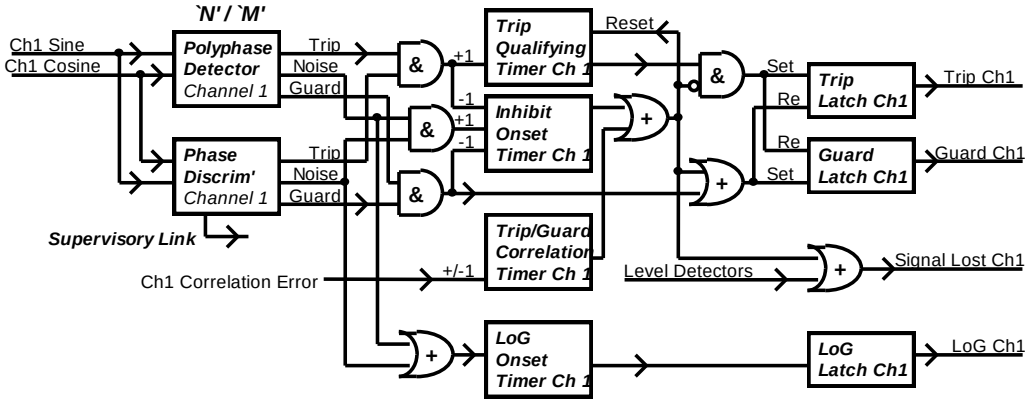


Figure 5.1 VF Trip Input Processing

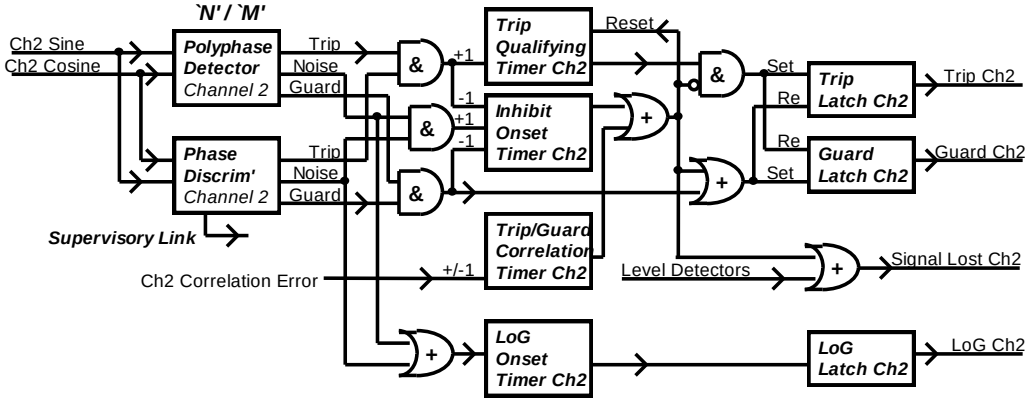
5.2 VF Trip Output Processing.

Refer figure 5.2a and 5.2b

- "Polyphase Detector" is a high speed phase shifting peak amplitude detector. The output from the "Polyphase Detector" is trip, guard or noise. The threshold points of the detector are controlled by user set values for ‘N’ / ‘M’. The setting for ‘N’ and ‘M’ for each trip command is independently set by the user. The detector is implemented by the uP.
- "Phase Discriminator" is a high speed quadrature phase detector. The output from the "Phase Discriminator" is a second set trip, guard or noise signals. The "Phase Discriminator" also detects supervisory link data (when enabled). The detector is implemented by the uP.
- "VF state decoder" provides the logical connections from the receiver trip and guard outputs to the trip and guard output sections. During “SIGNAL LOST” conditions the decoder applies the default output conditions as per the users setup, being “FORCE to GUARD”, “FORCE to TRIP” or “MAINTAIN OUTPUT”. The decoder also detects correlation errors in dual channel operation to cause the "Correlation Timers" to incremented on errors and decremented when no correlation error occurs. The decoder is implemented by the uP.
- "Trip Qualifying Timer" delays the trip output for a user set interval, of 0 to 250mS. The qualifying timer is used to check that the trip is stable through the interval. The timer is implemented by the uP.
- "Inhibit Onset Timer" delays the inhibit signal for a user set interval, of 0 to 250mS. The "Inhibit Onset Timer" delay the inhibit signal from inhibiting the trip output and forcing guard output, before sufficient time has elapsed to correctly determine the state of trip and guard outputs. When the "Inhibit Onset Timer" is reached, a user set interval for “Inhibit Extend” timer of 0 to 250mS is added to the "Inhibit Onset Timer" reset time. The extension gives the timer hysterisis, stopping small variations causing numerous inhibits. The timer is implemented by the uP. The "Trip Qualifying Timer" and the "Inhibit Onset Timer" settings are used in conjunction with each other to set noise security and response time in VF operation.
- "Correlation Timer" is used to detect VF channel differences in dual channel operation. The timer interval is a user set interval, of 0 to 250mS. When the timer interval is reached, an inhibit signal forces guard to be output. The "Correlation Timer" has an extension equall the “Inhibit Extend” added to the reset time. This extension gives the timer hysterisis, stopping short term correlation errors causing numerous inhibits. The timer is implemented by the uP.
- "hold off timer" stops multiple trips close together from being output before equipment connected to the "trip output interface" has had time to reset. The amount of hold off is setup by the user from 0 to 20 seconds. The "hold off timer" is implemented by the uP.
- "output extend timer" allows the duration of trip (or guard) transmission to be extended to allow short trip receptions to have enough time to operate. The timers are implemented by the uP. The amount of extension time is controlled by user setup from 0 to 990mS.
- the "termination timer" can be set to remove trip (or guard) signals after a time-out period set by the user from from 0 to 20 seconds. The "termination timer is implemented by the uP.
- "trip received counters" increment each time the trip changes to a one level and guard changes to a zero level. The counters are implemented by the uP, output to monitor module for display and storage.
- "trip output interface" combines the trip and guard signals. The output contacts close when the trip is a one level and the guard is a zero level.
- “LoG” (Loss of Guard) outputs a high speed signal via a second trip IO module. The output contacts close when the ‘in channel’ VF signals are lost for more than the “INHIBIT ONSET” time.



VF Receiver Channel 1 Output Section (Typical).



VF Receiver Channel 2 Output Section (Typical).

Figure 5.2a VF Trip Detector Processing (typical configuration)

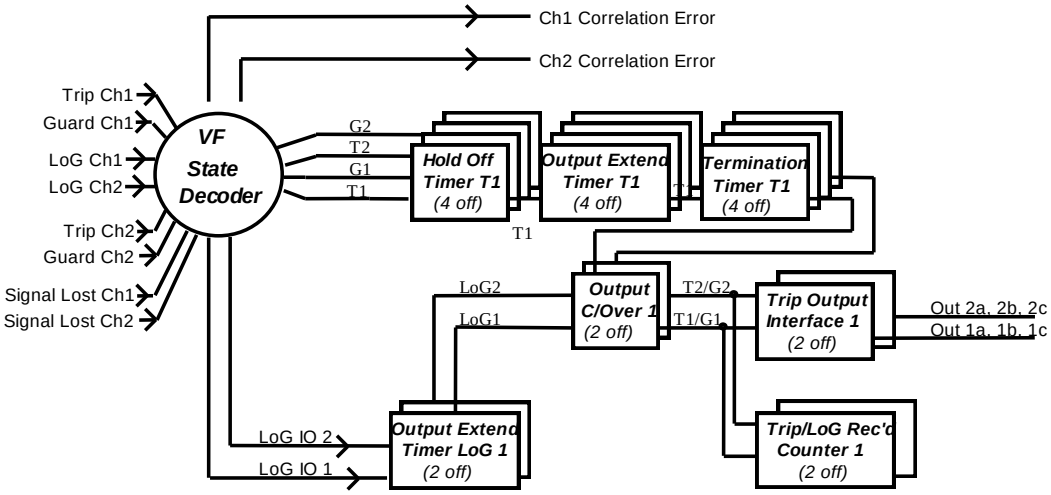


Figure 5.2b VF Trip Output Processing

6. G703 Processor Module.

Refer figure 6

- transformers and buffer amplifiers provide 500VDC electrical isolation for the 64 kilobaud data and clock signals. This allows the processor module circuitry to run at ground potential, ensuring safe electrical levels in processor operation.
- "TX EPLD" and the "RX EPLD" interfaces the co-directional and contra directional signals from the communication link to the DSP.
- "DSP" implements the user settings, self tests, trip input and trip output control functions.
- "monitor interface" provides a path for setup data from the monitor module, and operational data to the monitor module.
- "watchdog timer" ensures the DSP is running within the required time restraints. If DSP timing is not correct, indicating a possible software failure, the watchdog resets the DSP.
- "trip input / output interface" provides the signal driver to operate the trip IO cards.

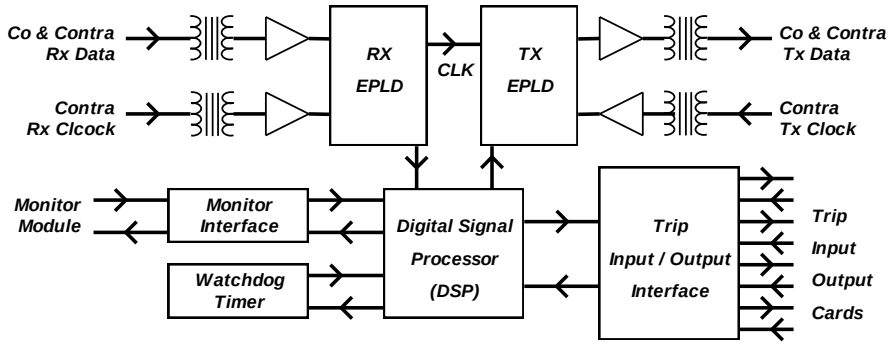


Figure 6 G703 Processor Module

7. RS422 Processor Module.

Refer figure 7

- RS422 line transceiver and opto' isolators provide 1000VDC electrical isolation for the data and clock signals. This allows the processor module circuitry to run at ground potential, ensuring safe electrical levels in processor operation.
- "TX EPLD" and the "RX EPLD" interfaces the co-directional and contra directional signals from the 64 kilobaud communication link to the DSP.
- "DSP" implements the user settings, self tests, trip input and trip output control functions.
- "monitor interface" provides a path for setup data from the monitor module, and operational data to the monitor module.
- "watchdog timer" ensures the DSP is running within the required time restraints. If DSP timing is not correct, indicating a possible software failure, the watchdog resets the DSP.
- "trip input / output interface" provides the signal driver to operate the trip IO cards.

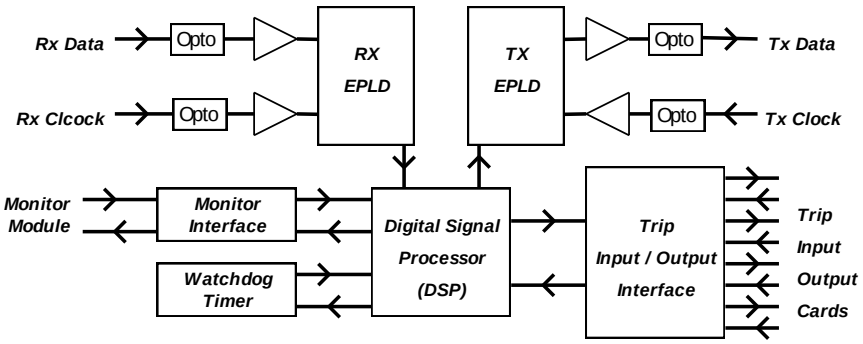


Figure 7 RS422 Processor Module

8. VF Processor Module.

Refer figure 8

- transformers and buffer amplifiers provide 5000VDC electrical isolation for the voice frequency (VF) send and receive pilots. This allows the processor module circuitry to run at ground potential, ensuring safe electrical levels in processor operation. The receive pilot AGC amplifier adjusts the levels into the receiver bandpass filters, stopping input levels causing distortion.
- "microcomputer" (uP) controls all aspects of the processor module's operation by implementing user settings, self tests, trip input and trip output control functions.
- "monitor interface" provides a path for setup data from the monitor module, and operational data (line levels and alarms) to the monitor module.
- "watchdog timer & EEPROM" ensures the uP is running within the required time restraints. If uP timing is not correct, indicating a possible software failure, the watchdog resets the uP. The EEPROM provides non-volatile storage for processor calibration data and a back up for user setup data, in case of monitor module failure.
- "trip input / output interface" provides the signal driver to operate the trip IO cards.
- "Ch#1 frequency generator EPLD" and "Ch#2 frequency generator EPLD " provide all frequencies for filter operation and the fundamental frequencies for transmission and reception. The frequency are locked to one quartz crystal, giving very stable operation.
- "IO buss controller EPLD" increases the data buss bandwidth available to uP without slowing the uP.
- "analogue interface circuits" digitises the "receiver quadrature signals" and pilot line levels for uP input.
- "VF transmitter 1" and "VF transmitter 2" generate the transmission VF sinewave frequencies. Each transmitter has a "level control" circuit and a 4th order bandpass filter. The uP controls the transmitters. The bandpass filters are digital programmed by the uP.
- "VF receiver 1" and "VF receiver 2" each filter required signals from the receive pilot using 8th order bandpass filters. An AGC amplifier adjusts the gain of each channel for output to the cosine / sine modulators. The cosine / sine modulator produces of sum and difference frequencies. The sum and difference frequencies are filtered low pass filters to produce quadrature outputs. The quadrature outputs are digitised by the "analogue interface circuits" for the uP decode trip and guard levels.
- The operating frequencies, and bandwidths can be setup from menus available in the monitor module. Each VF channel can have trip and guard frequencies set from 300 hertz to 4095 hertz in 1 hertz steps. The available guard to trip shift frequencies are from 20 to 500 hertz in 1 hertz steps. The transmitter and receiver bandpass widths can be set to user requirements.
  Please note that the CCITT G232 standard allows for operating frequencies from 300 hertz to 3400 hertz and the DM1200 VF processor module can operate upto 4095 hertz, if set to a non CCITT channel.

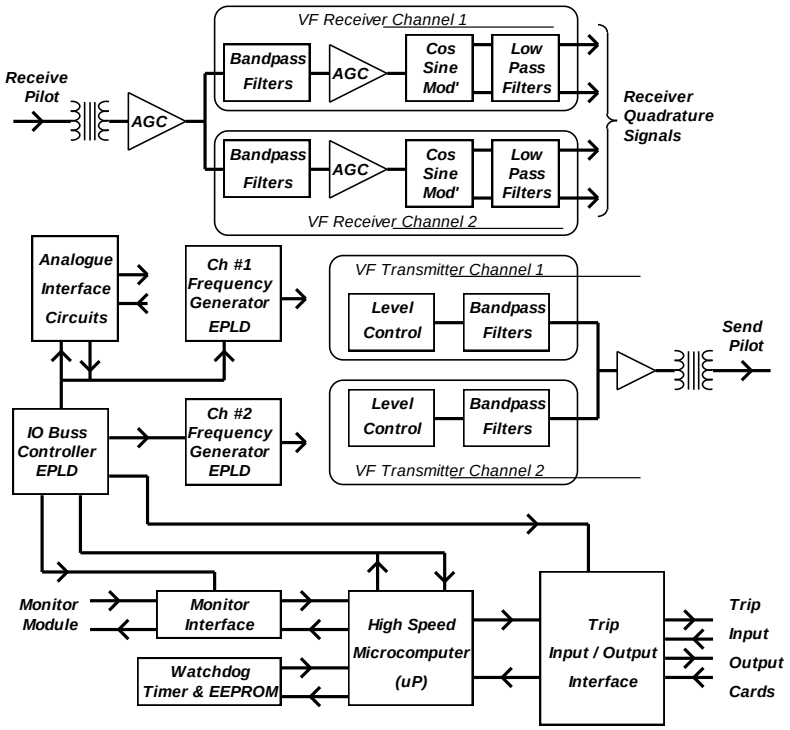


Figure 8 VF Processor Module

9. C37.94 Processor Module.

Refer figure 9

- optical tranceiver provide electrical isolation for the N times 64 kilobaud data and clock signals.
- “FPGA” interfaces the co-directional signals from the communication link to the DSP.
- "DSP" implements the user settings, self tests, trip input and trip output control functions.
- "monitor interface" provides a path for setup data from the monitor module, and operational data to the monitor module.
- "watchdog timer" ensures the DSP is running within the required time restraints. If DSP timing is not correct, indicating a possible software failure, the watchdog resets the DSP.
- "trip input / output interface" provides the signal driver to operate the trip IO cards.
- LOS (Loss of Signal) detection LED for user interface denoting the total loss of signal at local receiver.
- RDI (Remote Defect Indication) detection LED for user interface denoting the LOS of remote receiver.
- 7-segment LED display for indicating which optical transceiver module is being used at the local end.

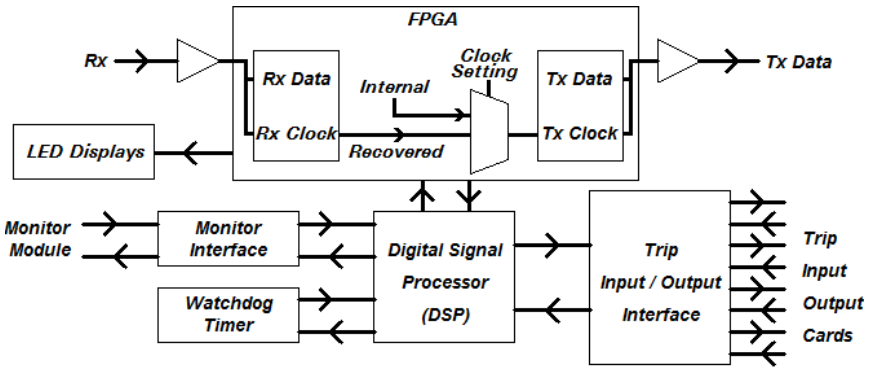


Figure 9 C37.94 Processor Module

10. Trip Input Output Module.

Refer figure 10

- each card handles one command function.
- up to four Trip I/O cards for Digital and up to two Trip I/O cards for VF may be fitted to the subrack.
- provides the barrier between the external trip circuits and internal logic.
- trip input voltage may be set by the user for trip battery voltages of 24, 32, 48, 120 and 240 V.
- three sets of trip solid state output 'contacts' are provided. The output contacts can be setup via the menu as normally open or normally close state.
- dual paths for both input and output are provided to ensure that a component failure cannot result in a false trip.

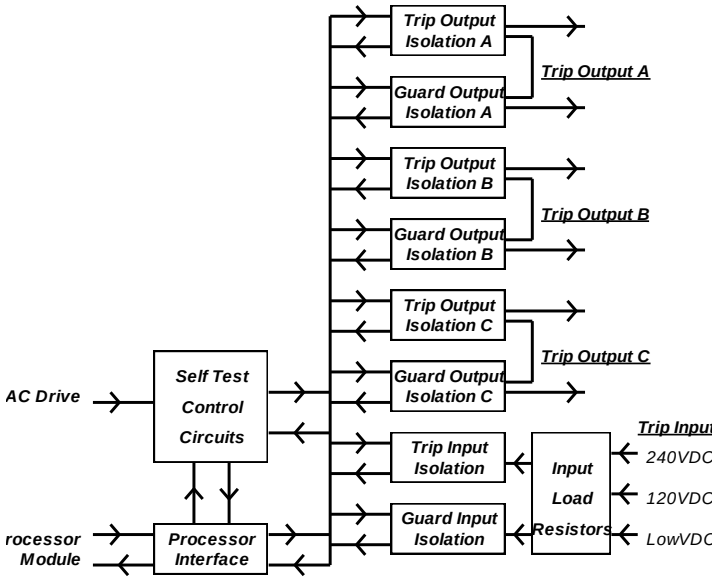


Figure 10 Trip IO Module

11. Power Supply Card.

Refer figure 11

- isolates the users communication battery from the system's internal rails to 5000VDC.
- contains the 'common alarm' relay and the VF boost input, both isolated to 5000VDC.
- available in two versions, one for nominal battery voltages of 20 to 60VDC, and 90 or 320VDC operation.
- inrush protection and ripple filtering ensure minimum disturbance to the users battery supply.

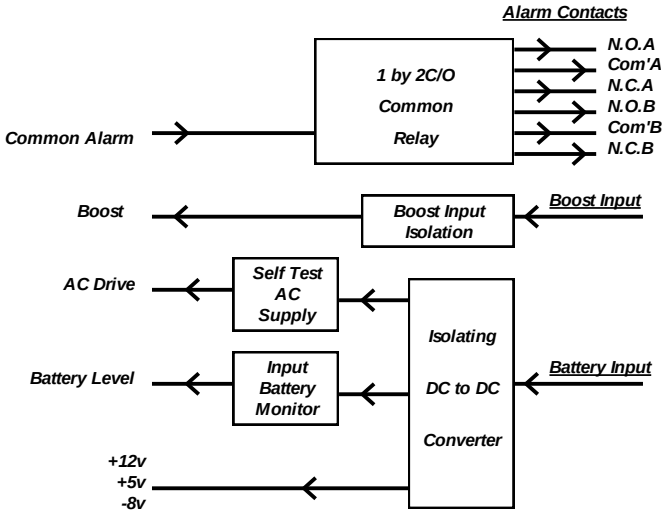


Figure 11 Power Supply Module

12. Monitor Module.

Refer figure 12
The Monitor module provides the operator with an interface to the system enabling the user to setup and test the DM1200 terimnal.

The operator interface consists of a menu driven 80 character, back-lit LCD display and six membrane switches. By scrolling through the display, information about the configuration and operational history of the system can be observed. Attention is drawn to alarm or trip activity by the flashing of the display back light. Access to monitor functions can be restricted by pass code and a setup change lock out in provided by an internal read only switch.

Typical of the items found in the setup menus are;

- Communications setup (ie G703, C37.94, RS422 or VF).
- Trip I/O configuration: Cards fitted, circuits used, trip input/output options.
- Security / dependability / reponse time.
- Timing: Input debounce, input and output extend times, forced termination time, hold-off time.
- Alarm and status: Allocation of relays, time delay, latching and on / off action.
- Trip counter reset: All or specific counters.
- Manual Test: Select trip test type, request permission, grant permission, test trip.

In order to signal alarm or status information, the Monitor module may be fitted with one or two relay cards, providing up to a total of 16 changeover contacts. In addition, RS232 serial port is provided enabling access via PC, laptop or modem. Adjacent terminals may be networked to eliminate the need for multiple serial links.

To help users maintain records the monitor module records last 1024 trip events and the last 1024 alarms events into 2 separate event logs. Each event (ei the on event and the off event) are time and stamped. The alarm event log also has a reason for the alarm stored in the event log (eg “ACCESS LCD” or “PSU WARNING +5”) where appropiate.

To aid in user setup, the monitor module conatins three complete sets default setup tables for the three most common applications, “HIGH SECURITY” (used for direct intertripping), “OPTIMUM” (used for permissive tripping) and “HIGH SPEED” (used for blocking).

In addition, the monitor module can check the setup being input against a user set performance requirement. If setup is wrong or inconsistent with the performance required, the parameter in question is displayed (eg “NO TRIP IO CARD#2 FITTED” or “QUALIFYING TIME TOO SHORT”).

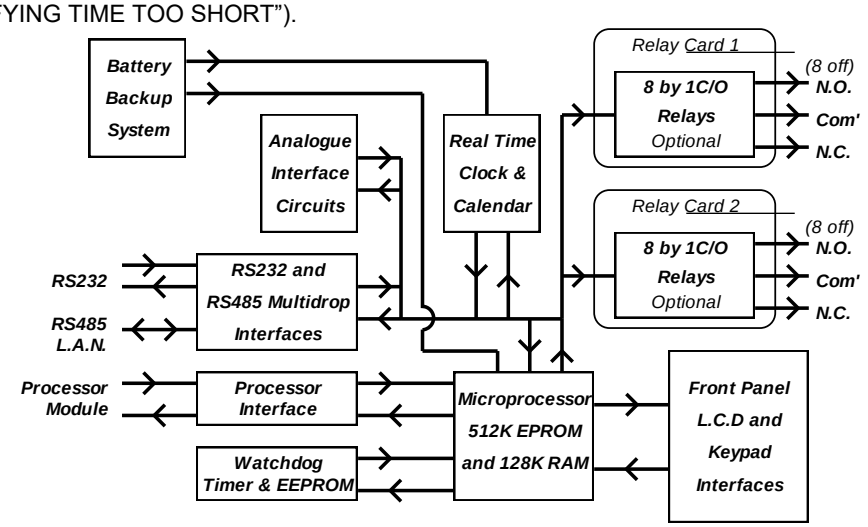


Figure 12 Monitor Module

13. Automatic Self Tests.

Trip input circuits are each tested from the input to the isolation optocouplers into the processor card. Each trip and guard signal from each trip IO cards is sequentially energised by an under threshold input and then energised by an over threshold level, testing each of the eight input signal paths with "go / no go" criteria. The self tests can also check the integrity of the trip input wiring by fitting a current bleed resistor across the “fault relay” contact.

Trip output circuits are tested in three ways. Firstly output discrepancy test circuits on the trip IO card detected shorted transistors on the output. If no shorted transistors are detected then the trip and guard transistors are turned on alternatively, checking that each transistor operates. The output self tests check the availability of supply to the trip output terminal, giving an open circuit alarm if the supply is less than 18 volts. This also checks the wiring integrity to the trip output.

The communications link is tested in a number of ways. The G703, C37.94 and RS422 links are tested by the processors each passing correct check bits in the data stream. The VF links are checked for frequency and level. The monitor module's supervisory link establishes communications with the remote end. The presence of this link operating correctly confirms operation.

Because of the built-in automatic testing, externally "time programmed" testing functions are not required.

14. Manual Tests.

Manual tests are provided via menu driven procedures.

- Live Test: Allows full trip output operation. For a live test trip transmission to take place, an operator is required at both ends, to setup the live test function. The live test can then be initiated by an operator pressing the trip button.
- Safe Test: Allows trip transmission, but the trips are not output. For a safe test trip transmission to take place, an operator is required at both ends, to setup the safe test function. The safe test can then be initiated by an operator pressing the trip button.
- Watch Inputs: This test allows user to check the operation of the trip input circuitry. During watch inputs testing, the trip signals are not transmitted.

15. General Data.

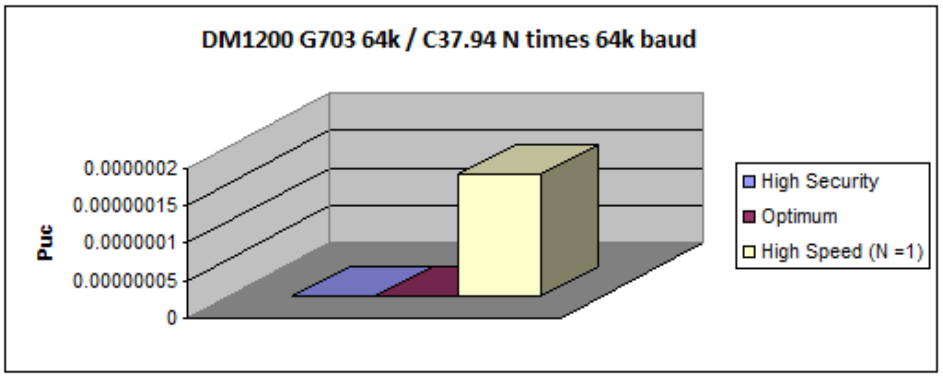
Power requirement		20 to 60V or 90 to 320V (Ordering option). 15W to 25W approx. depending on options.
Trip Command Input		User selectable nominal voltages of 24, 32, 48, 110 or 240, all -20% to +35%. For nominal voltage below 240V, nominal current is approx. 40mA with a guaranteed threshold of 30mA. At 240V the values are 20mA and 15mA. Input circuit integrity self test bleed current 20mA on 24 VDC to 110 VDC inputs and 10mA on 240 VDC input.
Trip Command Output		Three isolated 'contacts' rated at 2.0A @ 340V.
Command Counters		Up to 8 counters to record trips sent and received. plus LoG received
Command timers		Debounce time, input extend time, output extend time, hold off and cut off time.
Relays		Alarm / status relays: 8 or 16 C/O relays rated at 2A @ 48 VDC, 300mA @ 300VDC. Any alarm or status condition can be directed to any relay combination including common alarm relay. "ORing" of alarms is permissible. Relay time delay, latching or self resetting, and on or off alarm state can be user set.
G703 Communications		CCITT G703 64Kb/s, co-directional or contra-directional, and loop for testing.
RS422 Communications		9Kb/s to 80Kb/s master or slave clocking with clock inverts, and loop for testing.
C37.94 Communications		IEEE C37.94 N times 64Kb/s, internal clock, recovered clock, and loop for testing.
C37.94		
Module 1	Tx Output	-22.04dBm (short) / -17.79dBm (long)
	Rx Threshold[1]	-23.63dBm
Module 2	Tx Output	
	Rx Threshold	
Module 3	Tx Output	-13.01dBm
	Rx Threshold	-40.59dBm
VF		
VF Communications		User selectable extended CCITT G232 Voice frequencies from 300Hz to 4095Hz
VF Transmitter Output		-35dBm to +3dBm per channel
VF Receiver Sensitivity		-40dBm to +10dBm total line level
Self test		All input/output and communication functions under continuous test.
Withstand, HFD and Isolation		Power supply, trip input, trip output and common alarm relay to IEC 255 Class III.
Connections		All termination at rear on plug in terminals. Suitable for 2.5 sq. mm cable. Plug-in mating connector supplied.
Physical Size		19 inch 3 U high rack mounting. Depth 355 mm.
Mounting		Flush or semi projection mounting.
Weight		6.2Kg.approx. (depending on modules fitted).
Shipping weight		7.5Kg (maximum)

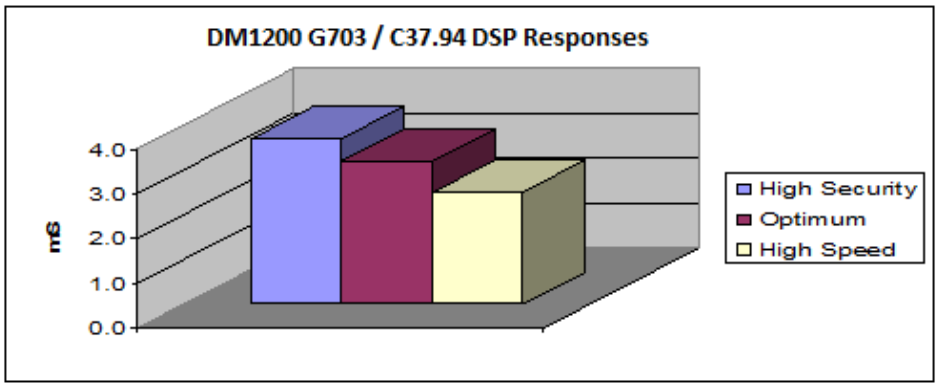
[1]Rx threshold is not measured for the receiver module's sensitivity, but rather as the last power level measured before the unit shows "10000" BER (the threshold BER).

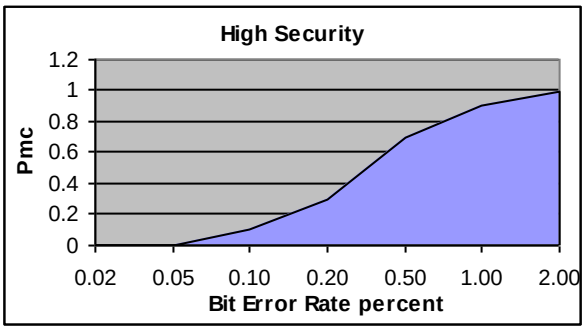
15.1 Typical Performance.

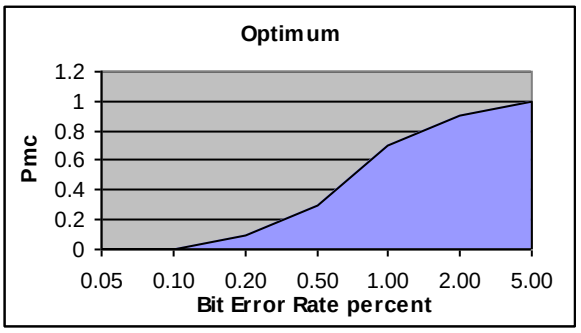
The following charts show typical performance data using the inbuilt default setup tables.

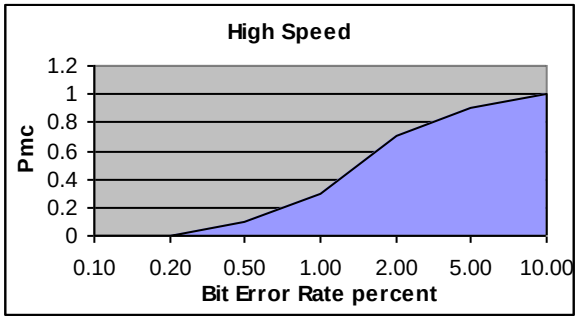
15.1.1 Typical G703 / C37.94 Performance.



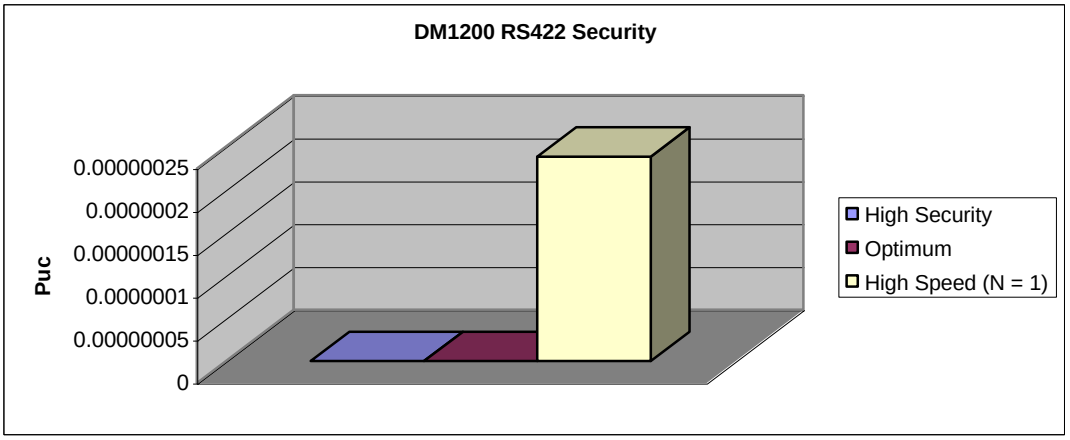


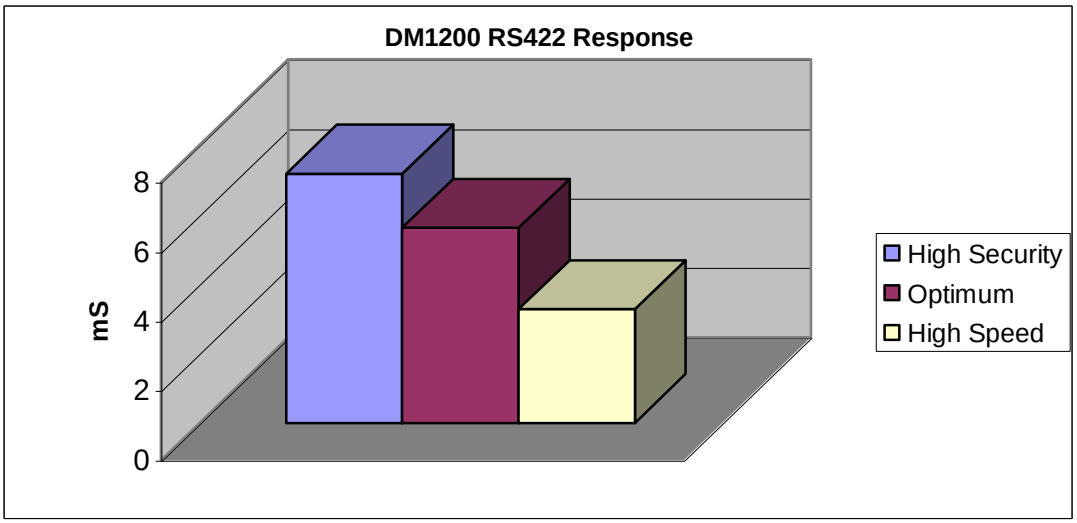


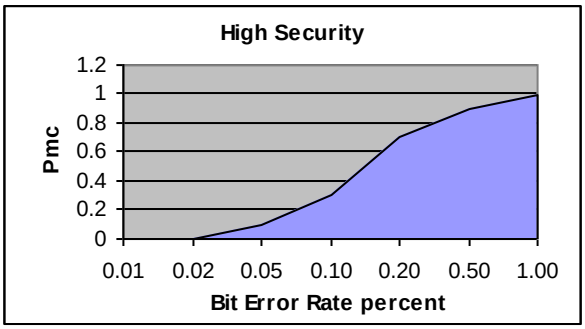


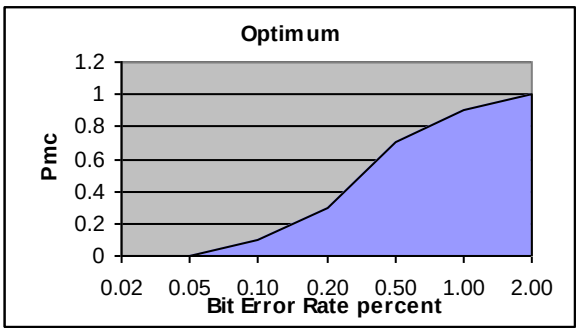


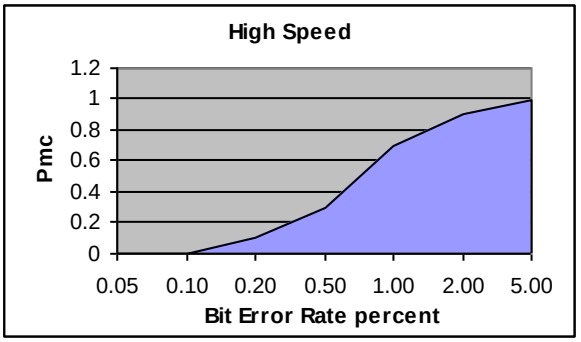
15.1.2 Typical RS422 Performance.



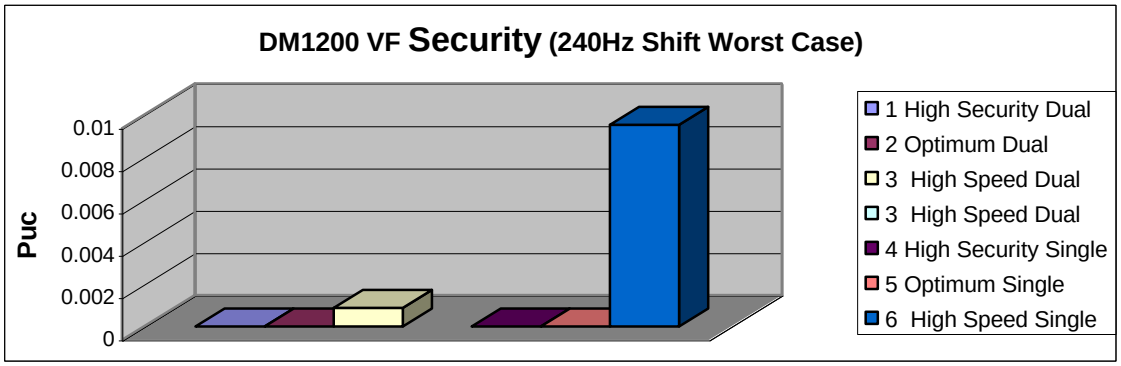


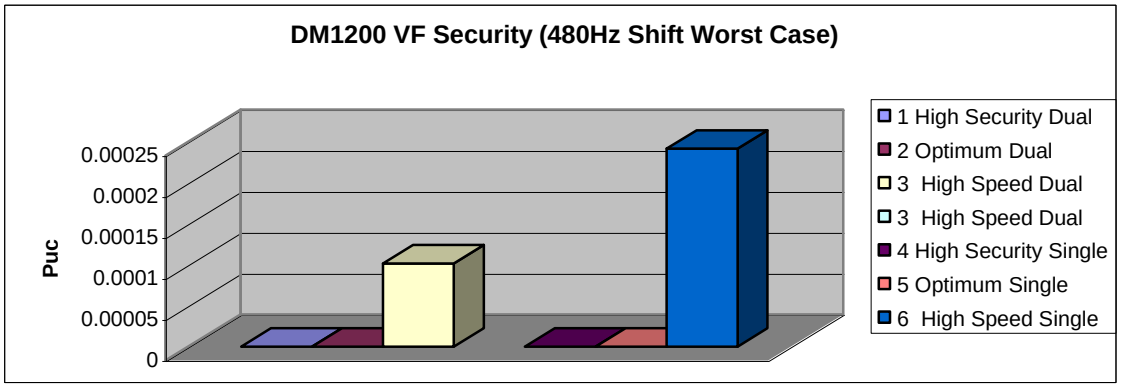


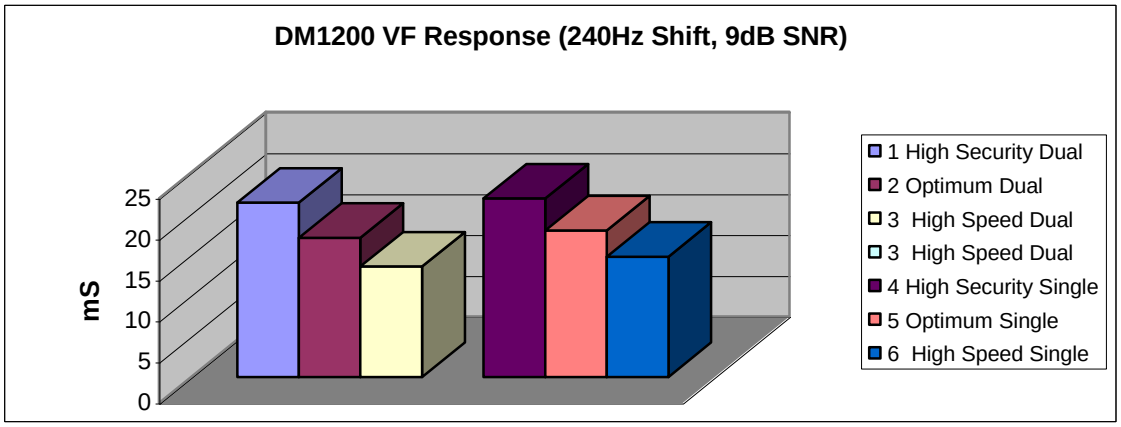


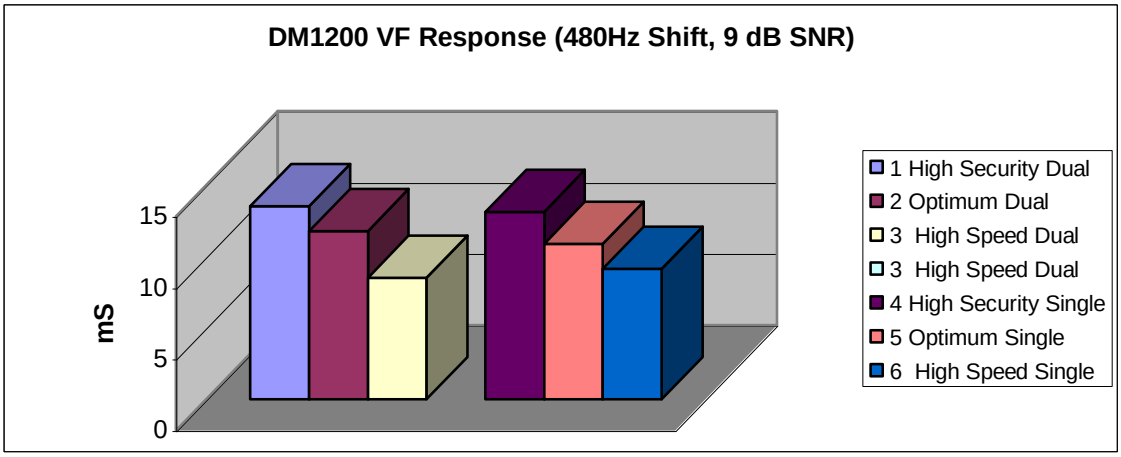


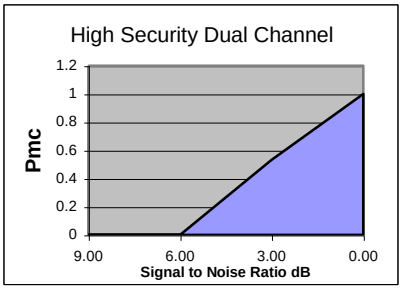
15.1.3 Typical VF Performance.







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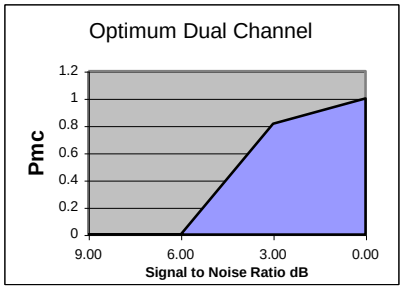
Signal to Noise Ratio dB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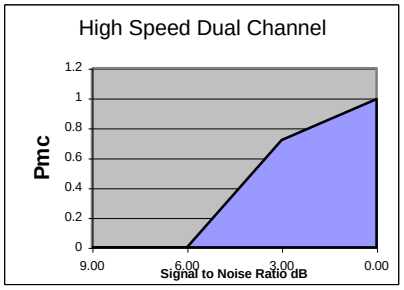
Signal to Noise Ratio dB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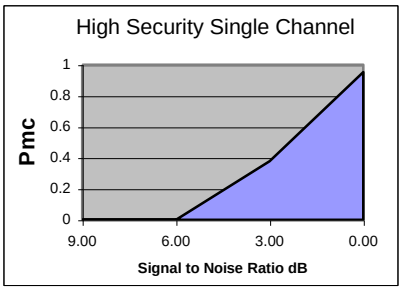
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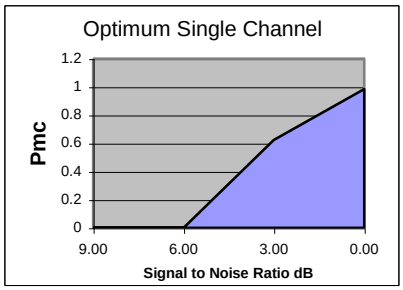
Signal to Noise Ratio dB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6.00
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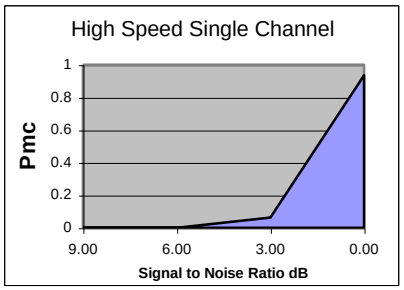
0.00
Signal to Noise Ratio dB


High Speed Single Channel
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0.4
0.2
0
9.00
6.00
3.00
0.00
Signal to Noise Ratio dB

15.2 List of Terminal Alarm Conditions.

RECD SIGNAL LOSS	No receiver signal on G703 or RS422.
AIS CONDITION	Mux' has sent "all ones" on G703 or RS422.
HIGH BIT ERROR	Bit error rate high on G703 or RS422.
#1 INPUT FAULT	Trip 1 input circuit failed.
#2 INPUT FAULT	Trip 2 input circuit failed.
#3 INPUT FAULT	Trip 3 input circuit failed on G703 or RS422.
#4 INPUT FAULT	Trip 4 input circuit failed on G703 or RS422.
OUTPUT S/C FAULT	Trip output has a short circuit.
#1 OUT O/C FAULT	Trip 1 output has an open circuit.
#2 OUT O/C FAULT	Trip 2 output has an open circuit.
#3 OUT O/C FAULT	Trip 3 output has an open circuit on G703 or RS422.
#4 OUT O/C FAULT	Trip 4 output has an open circuit on G703 or RS422.
PSU WARNING	Power supply voltage is out of tolerance or the subrack temperature is out of tolerance.
#1 FORCED CUT-OFF	Trip 1 terminated by time-out.
#2 FORCED CUT-OFF	Trip 2 terminated by time-out.
#3 FORCED CUT-OFF	Trip 3 terminated by time-out on G703 or RS422.
#4 FORCED CUT-OFF	Trip 4 terminated by time-out on G703 or RS422.
#1 HOLD-OFF ALARM	Another trip 1 occurred during hold off time.
#2 HOLD-OFF ALARM	Another trip 2 occurred during hold off time.
#3 HOLD-OFF ALARM	Another trip 3 occurred during hold off time on G703 or RS422.
#4 HOLD-OFF ALARM	Another trip 4 occurred during hold off time on G703 or RS422.
REMOTE ALARM	Remote Communications failure or alarm.
MONITOR FAULT	Monitor alarm, setup failures.
PROCESSOR FAULT	Teleprotection processor failure.
OFF NORMAL	Terminal "OFF NORMAL" (e.g. setup, test, etc).
#1 SENT	Trip 1 being sent, slow speed copy.
#2 SENT	Trip 2 being sent, slow speed copy.
#3 SENT	Trip 3 being sent, slow speed copy on G703 or RS422.
#4 SENT	Trip 4 being sent, slow speed copy on G703 or RS422.
#1 RECD	Trip 1 being received, slow speed copy.
#2 RECD	Trip 2 being received, slow speed copy.
#3 RECD	Trip 3 being received, slow speed copy on G703 or RS422.
#4 RECD	Trip 4 being received, slow speed copy on G703 or RS422.
POWER FAIL	Power failed alarm (for recording in event logs).
IDENT FAIL	Terminal to terminal Identity Alarm
TRANSMITTER ALARM	Transmitter fail (VF processor only).
RECEIVER ALARM	Receiver fail (VF processor only).
INHIBIT ALARM	Trip out inhibited (VF processor only).
ACCESS ALARM	Terminal menus being accessed
COMMON ALARM	Used as a substation alarm, can be any combination of the above alarms.
REMOTE BOOST INPUT	Slow signal from the remote DM1200 terminal's "BOOST INPUT"

NOTE: Any of the above alarm conditions can be setup by the user to activate any alarm relay.

15.3 DM1200 System Identification.

See **313-010 DM1200 System Configuration** Sheet for the details.

INDEX

LIST of FIGURES