DEWAR ELECTRONICS

DM 1200 Series Teleprotection

Dewar Electronics Pty Ltd.
32 - 34 Taylors Road, Melbourne, Croydon,
Victoria, Australia. 3136
Phone +61 3 9725 3333, Fax +61 3 9725 6003
Email: sales@dewar.com.au, Home Page: www.dewar.com.au

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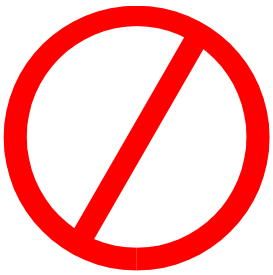

WARNING

LITHIUM BATTERIES

DEWAR DM1200 TELEPROTECTION TERMINAL CONTAINS A LITHIUM BATTERY.

DANGER OF EXPLOSION EXISTS IF THE BATTERY IS INCORRECTLY REPLACED

REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER.

LITHIUM REACTS VIOLENTLY WITH WATER AND MOST GASES AND SHOULD NOT BE CRUSHED OR INCINERATED.

WARNING

COMPATIBILITY

THIS MANUAL IS INTENDED FOR USE ON DM1200 TERMINALS WITH;

1200-10B	**MONITOR HARDWARE WITH FIRMWARE V6.00 OR HIGHER,**
1200-12	**RELAY CARDS,**
1200-21	**G703 PROCESSOR WITH FIRMWARE V3.10,**
1200-22	**VF PROCESSOR WITH FIRMWARE V5.12 OR HIGHER,**
1200-32	**TRIP IO MODULE,**
1200-42, -43	**POWER SUPPLY MODULES,**
1200-50	**SUBRACK AND MOTHERBOARDS,**
DM1200TALK	**OPTIONAL TERMINAL ACCESS SOFTWARE V6.00 OR HIGHER.**

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Introduction

Teleprotection is defined as "protection of a circuit, the ends of which are geographically separate, eg. Lines and cables, in which cooperation is obtained between the two relaying points by the transmission of information over the distance by telecommunication techniques.

The **DEWAR DM1200** not only meets this need but by the use of the latest digital technology and software control, have established new benchmarks in user convenience, performance, reliability and features.

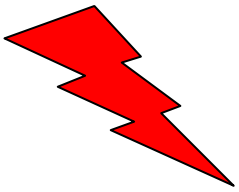
The **DEWAR DM1200** is available in several standard configurations (refer appendix E). Being software based, the **DEWAR DM1200** also provides the opportunity to program user specific requirements via menus through soft touch keypads.

The **DEWAR DM1200** is the latest teleprotection system in a long pedigree of teleprotection systems. The DM1200VF system is pilot line compatible with all previous DEWAR teleprotection models including 631, 650, 685, 685U and 695.

This manual provides the user with all the information needed to install, operate and maintain their systems.

Important Messages

Users are advised to pay particular attention to any paragraph marked with the following:-



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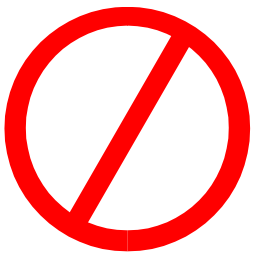

***** WARNING *****

Failure to observe these paragraphs may result in injury to personnel, incorrect operation or damage to the equipment.

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SECTION 1

Product Description

Features

The use of modern VLSI digital techniques has resulted in a compact unit with capabilities far exceeding those of previous models.

- Year 2000 compliant.
- Firmware control. Menu driven software control. Dual microprocessor architecture.
- All major system parameters under user control.
- Separate user pass-code entry to set up, maintenance and operations menus.
- User programmable security and dependability to suit user application.
- Non-volatile EEPROM set up storage. Duplicated write operations are stopped to extend EEPROM life.
- End to end supervisory link allows remote terminal identification, time locking, testing, etc.
- High speed 64Kbit/s communications; direct terminal to terminal or co-directional or contra-directional CCITT G703 digital link or CCITT G232 voice frequency processors.
- Input to Output utilises total dual path hardware and software redundancy (dual complimentary path) ensures that no single component failure can cause a trip.
- Continuous automatic self test (8 times per second) and Manual test. Self diagnostics to component level
- 4 by 20 character LCD and keypad provides full set up and monitoring facilities. No internal trimpots or adjustments. No add on requirements for programming.
- Supervisory link allows remote terminal identification, time locking, testing, etc.
- An RS232 / RS485LAN for remote supervision and set up via a PC or modem connection.
- Time stamping of command and alarm events. History of previous events with down load capability. Non volatile battery backed memory. Rechargeable backup battery
- An RS232 / RS485LAN for remote supervision and set up via a PC or modem connection.
- Power Supply modules, 20 to 60VDC or 90 to 320VDC,
- 1 or 2 Alarm Relay cards (8 by 1C/O relays per card) can be fitted.
- The G703 processor module can operate 1, 2, 3 or 4 trip IO cards giving 1 to 4 independent trip command functions.
- The VF processor module has two FSK channels. These can be configured as a dual channel single command high security system requiring 1 trip IO card, as a single channel single command system requiring 1 trip IO card or as 2 channel 2 command system requiring 2 trip IO cards. A fast Loss of Guard (LoG) output can be selected for interface to trip breaker logic.
- Alarms can be logically "ORed" to any relay and a pair of relays can be programmed to operate as a dual changeover. The alarm relays are provided in groups of 8. For 16 alarm relays, two relays cards are required. Also a common alarm relay, on the power supply card, can be programmed to operate with any alarm combination.
- Three separate command input voltage terminals 240VDC, 120VDC and a LOW voltage range. The LOW voltage can set to 24, 32 or 48VDC with a jumper setting on the trip IO card.
- Three normally open command output "contacts" per command channel. Two trip output ranges are available, 2amp 320VDC maximum.
- Two power supply ranges are available, 20 to 60VDC and 90 to 320VDC, as an ordering option.
- Both the DM1200 and the DM1200VF systems are housed in a standard 3U by 19 inch terminal. As both systems use the same terminal and support modules, changing from VF to digital communications or vice-versa is achieved by simply changing of the processor module. The software for both G703 and VF is co-resident.
- Isolation, Impulse and HFD to IEC384-1 and IEC255 standards.
- Dust proof , 3U by 19 inch terminal enclosure.
- Checking the source identity of received signals on the G703 and VF communications channels.

1.1 Terminal Components.

1.1.1 Standard Terminal.

The 19", 3U high terminal houses the circuit modules and the Monitor module that comprise the **DEWAR DM1200.**. All wiring is to the rear of the unit via robust plug-in terminal blocks that may be pre-wired. This simplifies both installation and maintenance. A two level back plane arrangement separates the functions of field connections and internal signals thus protecting the equipment from accidental damage and interference.

All active components are mounted on keyed circuit cards that are accessible from the front of the terminal.

Reversible mounting brackets provide for either flush mounting in the user's rack or where depth is restricted, projection mounting. Provision is made for the user to fit a 'Tally Plate' to the top of the terminal.

1.1.2 Power Supply Card.

This card isolates the users communication battery from the system's internal rails. It also contains the 'common alarm' relay isolated to 5KV. The Power supply is provided in two versions, one for nominal battery voltages of 24V or 48V, the other for 110V or 240V operation.

Inrush protection and ripple filtering ensure minimum disturbance to the user's battery supply.

1.1.3 G703 Processor Card.

This card performs the real time tasks required by the system for 64kB G703 communications. It uses a Digital Signal Processor (DSP). The tasks include:

- Communications with remote terminal.
- Communications with the monitor module.
- Debounce of the trip-input signal from the field.
- Validity tests on received signal from the remote terminal.
- Timed extensions on the trip command.
- Self testing of the command IO hardware.
- Provide a supervisory data path for monitor to monitor communication.

1.1.4 VF Processor Card.

This card performs the real time tasks required by the system for voice frequency communication. It uses a microprocessor and switched capacitor filter technology. The tasks include:

- two FSK transmitters and two FSK receivers.
- communications with remote terminal.
- communications with the monitor module.
- Debounce of the trip input signal from the field.
- frequency analysis on the received signal from the remote terminal.
- timing functions related to noise and command security.
- timed extensions on the trip command.
- self testing of the command hardware.
- provide four tone FSK to encode and decode supervisory data for monitor to monitor communication.
- Provide Loss of Guard (LoG) detection.

1.1.5 Trip I/O Card.

This card provides 5000 volt isolation barrier between the command field wiring and rest of the system. The command input voltage is selected by the user for command battery voltages between 24V and 240V. Three sets of command output 'contacts' are provided. Dual path circuitry for both input and output are provided to ensure that a component failure cannot result in a false trip.

Up to Four Trip I/O cards may be fitted to the terminal for G703 communication and up to two trip IO cards fitted for VF communications.

1.1.6 Monitor Module.

The Monitor Module provides user interface to the terminal and provides extensive alarm reporting and monitoring facilities. The Monitor Module can interface with one or two relay cards, providing a maximum of 16 single changeover contacts, for the external signalling of alarm and command activity.

The operator interface consists of an 4 line by 20 character, back-lit LCD display and membrane switches. By scrolling through the display, information about the configuration and operational history of the system can be observed. Attention is drawn to alarm or command activity by the flashing of the display back light.

The Monitor Module provides communication between both terminals during manual trip testing and a means to change the operating mode or adjustments. Typical of the items found in the menus are;

Supervisory functions
- local terminal status,
- remote terminal status,
- processor control,
- identity checking,
- power supply checking.
- alarm processing,
- alarm relay control,
- set-up menus,
- logs for command and alarm event history,
- local area network between terminals
- answer only modem interface to the public telephone network,

Communication Mode
- processor type,
- trip and guard frequencies over VF link,
- Co or contra-directional over G703 link,
- master / slave over G703 link,
- Local loop back for testing.

Trip I/O configuration
- cards fitted, circuits used.

Security level
- count of valid frames on G703.
- qualifying time, inhibit onset time, correlation time and inhibit extend time.
- transmitter and receiver output options on VF.

Trip IO Timing
- input de-bounce, input and output extend times, forced cut-off time, hold-off time.

Alarms
- allocation of relays, on-set time delay, latching or non-latching action.
- common alarm control.

Trip Counter Reset
- all or specific counters.

Manual Trip
- request permission, grant permission, select trip circuit.

The Monitor has a RS232l port enabling communication with external devices.

Access to certain functions is restricted by pass codes. These codes can be set by the user or left set to 0000 for unrestricted access if so desired.

1.2 Security.

The security of a system against the generation of false trips as a result of communication faults, noise or crosstalk is a trade off against speed of operation and dependability.

1.2.1 G703 Security and Dependability.

Within G703 communication, the delay is short so that only the security/dependability trade-off need be considered. This trade-off is set by specifying the number of uncorrupted words that must be received within a nominated window.

The use of error detecting line codes and sequential frame numbering enables the detection of data which has been corrupted by abnormalities such as bit errors, synchronisation slip, foreign signal sources and noise. As an option, terminals may be ‘paired' together using end to end identity checking, to protect against the possibility of crossed communication channels.

The security is set up by selecting 'N' valid frames out of 'M' consecutive frames.

The value of ‘M’ sets the security sampling period to ‘M’ times 0.5 milliseconds. The range of ‘M’ values can be from 1 to 16.

Increasing the value of 'N' increases security and increases response time by 'N' times 500 microseconds. The range of 'N' can be from 1 to the value of 'M'. 'N' cannot be greater than 'M'.

G703 guard to trip response time can be calculated as follows;-

Response time = T_{IP} + T_{CT} + ('N' * 0.5mS) + T_{OP}

Where;

T_{IP} = input processing delay = the greater of 0.5mS or debounce time (see Input/Output Security),

T_{CT} = external communications delay between the two DM1200 terminals,

'N' = set value,

T_{OP} = output processing delay = 0.5mS,

Response Tolerance is +0.5mS, 0.0mS.

G703 trip to guard response time can be calculated as follows;-

Response time = T_{IPEXT} + T_{CT} + (('M' - 'N') * 0.5mS) +0.5mS+ T_{OPEXT}

Where;

T_{IPEXT} = input extend time setting,

T_{CT} = external communications delay between the two DM1200 terminals,

'N' and 'M' = setting values,

T_{OPEXT} = output extend tine setting,

Response Tolerance is +0.5mS, 0.0mS.

'M'	'N'	Security	Dependability	Comments
16	1	Lowest	Highest	Suitable for high speed blocking
16	16	Highest	Lowest	Not recommended. Any G703 bit error will cause a drop out during trip operation.
1	1	Low	High	Not recommended. Trip output can fluctuate during G703 bit errors.
8	6	High	Low	Suitable for direct tripping
8	4	Medium	Medium	Suitable for permissive tripping (default setting) (Passes the CIGRE bit error tests.)
8	2	Low	High	Suitable for blocking.

Table 1.2.1, Examples of G703 Security and Dependability

From table 1.2.1, the ratio of 'N'/'M' is the important factor when setting security/dependability for an application. An 'N'/'M' factor equal to 1 is not recommended. Settings suitable for blocking systems (high dependability) are when 'N'/'M' equals 0.25 or less. Settings suitable for permissive tripping systems (optimum security/dependability) are when 'N'/'M' equals 0.25 to 0.75. Settings suitable for direct tripping systems (high security) are when 'N'/'M' equals 0.75 or greater.

1.2.2 VF Security and Dependability.

The **DEWAR DM1200VF** set up menus allow the user to set the VF frequencies, bandwidths, N, M, command qualifying time, inhibit onset time, inhibit extend tine, correlation time and the method of application of the inhibit to trip operation used. Using these menus, the user can tailor the VF system requirements for speed, security and dependability to suit the teleprotection application required.

Security is set up by selecting values for qualifying time, inhibit onset time, correlation time, receiver output options, 'N', 'M' and single / dual channel operation.

The range of values for 'N' and 'M' is the same as for G703 operation. (Refer section 1.2.1)

Increasing the qualifying time, and 'N'/'M' factor increases security and increases the response time.

Using dual channel (using both transmitters and both receivers for one command) operation increases security, but limits the commands per VF terminal to one. Using single channel (using one transmitter and one receiver for one command) operation has reduced security, but allows two commands per terminal.

Decreasing inhibit onset time and increasing inhibit extend time increases security and decreases dependability.

Increasing bandwidth (and FSK frequency shift) decreases response time.

Minimum VF guard to trip response time can be calculated as follows: -

Response time $= T_{IP} + T_{TXGD} + T_{TXOP} + T_{CT} + T_{RXIP} + T_{RXBP} + T_{RXLP} + T_{RXDETECT} + T_{QUALIFYING} + T_{OP}$

Where;

- T_{IP} = input delay, which is the greater of 0.69mS or debounce time (see Input/Output Security),
- T_{TXGD} = transmitter group delay = 0.46mS,
- T_{TXOP} = transmitter output delay = 0.01mS,
- T_{CT} = external communications delay between the two DM1200VF terminals.
- T_{RXIP} = receiver input delay = 0.02mS,
- T_{RXBP} = receiver band pass delay = the greater of 0.92mS or 1/(receiver pass band setting),
- T_{RXLP} = low pass filter group delay = 1/(FSK frequency shift),
- $T_{RXDETECT}$ = receiver detection delay = ('N' / 'M' + 0.25)/(FSK frequency shift),
- $T_{QUALIFYING}$ = qualifying delay, user set value,
- T_{OP} = output delay, which is 0.69mS,

Response Tolerance is dependent on a number of other set up options. All

Minimum VF trip to guard response time can be calculated as follows: -

Response time $= T_{IPEXT} + T_{TXGD} + T_{TXOP} + T_{CT} + T_{RXIP} + T_{RXBP} + T_{RXLP} + T_{RXDETECT} + T_{OPEXT}$

Where;

- T_{IPEXT} = input extend time setting,
- T_{TXGD} = transmitter group delay = 0.46mS,
- T_{TXOP} = transmitter output delay = 0.01mS,
- T_{CT} = external communications delay between the two DM1200VF terminals.
- T_{RXIP} = receiver input delay = 0.02mS,
- T_{RXBP} = receiver band pass delay = the greater of 0.92mS or 1/(receiver pass band setting),
- T_{RXLP} = low pass filter group delay = 1/(FSK frequency shift),
- $T_{RXDETECT}$ = receiver detection delay = ('N' / 'M' + 0.25)/(FSK frequency shift),
- T_{OPEXT} = output extend time setting,

Response Tolerance is dependent on a number of other set up options. All

Various other factors can effect VF response time, including noise and the settings for "Poly Averaging" and "Poly Phase Leads" as follows;-

A signal to noise ratio (SNR) of 6dB or greater has little or no effect on the response time. However signal to ratios less than 6dB will extend the response time exponentially as the SNR reduces. A SNR = 3dB will extend the response time by 2 to 4 times 1/(FSK frequency shift).

Selecting "Poly Phase Leads", removes the second phase from trip and guard state detection. This has the effect of maintaining response times at the minimum value between consecutive trips.

Selecting "Poly Averaging", causes the receiver signal processing to average the output sampling. This extends the response time by 0.25/(FSK frequency shift), but has the effect of keeping the response times closely matched between consecutive trips.

NOTE: Both "Poly Averaging" and "Poly Phase Leads" are recommended for distance acceleration tripping systems.

VF security and dependability (typical) for one command using both transmitters and both receivers

240 Hertz FSK shift	Qualifying, Inhibit Onset, Inhibit Extend Times	'N' / 'M'	False trip from noise burst	Dependability (as missed trips) at 6dB SNR	Description
Blocking	3, 8, 50 mS	2 / 8	< 1 trip in 10^3	< 1 missed in 10^6	High dependability, low security, high speed[6]
Permissive	5, 4, 50 mS	4 / 8	< 1 trip in 10^5	< 1 missed in 10^5	Medium dependability, security and speed[6]
Direct trip	7, 4, 50 mS	6 / 8	< 1 trip in 10^6	< 1 missed in 10^4	Low dependability, High security, Slow speed[6]

Table 1.2.2.1, Daul Channel VF Security

VF security and dependability (typical) for one command using one transmitter and one receiver;-

240 Hertz FSK shift	Qualifying, Inhibit Onset, Inhibit Extend Times	'N' / 'M'	False trip from noise burst	Dependability (as missed trips) at 6dB SNR	Description
Blocking	4, 10, 50 mS	3 / 8	< 1 trip in 500	< 1 missed in 10^7	High dependability, low security, high speed[6]
Permissive	6, 5, 50 mS	5 / 8	< 1 trip in 10^4	< 1 missed in 10^6	Medium dependability, security and speed[6]
Direct trip	10, 6, 50 mS	7 / 8	< 1 trip in 10^5	< 1 missed in 10^5	Low dependability, High security, Slow speed[6]

Table 1.2.2.2, Single Channel VF Security

Qualifying time is the main user setting for security in a VF system. Values equal to or greater than 4/(FSK frequency shift) give the highest security. Values less than 0.75/(FSK frequency shift) give the lowest or nil security. The qualifying time should be between these two extremes.

Inhibit onset time is the main user setting for dependability (higher inhibit onset times give high dependability). It also has an effect on security if the inhibit onset time is greater than the qualifying time. Inhibit onset time should be greater than 0.75/(FSK frequency shift), with inhibit detect width set to "Wide" or greater than 0.6/(FSK frequency shift) with inhibit detect width set to "Narrow". Setting inhibit on-set time to less than these values may result in an inhibit being generated by normal trip operation.

The inhibit extend time has an effect on security during high noise or repetitive noise bursts. If the extend time is longer, it will tend to continuously generate an inhibit, by treating the noise as one contiguous block of time. Trip operation is not available during inhibit extend time. The "Inhibit to Guard" setting can be turned off, but doing so will reduce security.

1.2.3 Input / Output Security.

There are other sources of poor security that are often given insufficient consideration. One of these is the command input circuit where unwanted signals can be induced. The **DEWAR DM1200** has a threshold of current which must be exceeded for an adjustable `debounce' time (to suppress spikes), before a trip is accepted.

1.2.4 Component Failure.

Another source of insecurity is component failure. The **DEWAR DM1200** has dual signal paths that commence after the trip input dropping resistors and continue right to the trip output terminals. These paths incorporate opto-isolators, microprocessor I/O ports, software functions and memory locations, code words and output transistors. The components used for the two paths do not share common packages and signal levels are complimentary. Both paths must operate to generate a trip, the fail-safe condition being guard.

Such redundancy is of limited value unless component failure can be detected. For this purpose the **DEWAR DM1200** self test routines provide continuous automatic detection of failed components in the command signal path.

1.2.5 Terminal Identity.

The **DEWAR DM1200** provides a facility to give security against the possibility of cross connection of communications bearers by checking the source identity of received signals on the G703 and VF communications channels. If identity checking is enabled, the Operations Menu pass codes (see Section 4.3) of both terminals must match before command operation is enabled by the monitor modules.

1.3 Firmware Version Compatibility.

***** WARNING ***.**

The major firmware version number, as read from the MENU, (the number to the left of the point) should be the same between monitor modules on both the local DM1200 terminal and the remote DM1200 terminal.

Firmware version checking takes place internally. If version differences occur, the monitor modules adjust their responses to the local processors and the remote monitors. In some cases the lower version can not interpret a request. In these cases the monitor module will display a message indicating that the operator request cannot be initiated. If a VF processor has a higher major version number than the monitor, the VF processor sets its version number to the major version number of monitor and appends ".99". If this happens it is recommended the Firmware be upgraded to the same version numbers between terminals. The version numbers for both local and remote Monitors and Processors can be displayed in the INFORMATION menu, TERMINAL DETAILS, GENERAL.

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SECTION 2

Specification.

Capacity: Four independent commands on G703, two independent commands on VF.

Power: 20 to 60V or 90 to 320V (Ordering option). 15W to 25W approx. depending on options.

Trip Input: User selectable nominal voltages of 24, 32, 48, 110 or 240, all -20% to +35%. For nominal voltage below 240V, nominal current is approx. 40mA with a guaranteed threshold of 30mA. At 240V the values are 20mA and threshold of 15mA.

Trip Output: Three isolated relay contacts. Rated at 2.0A @ 340V maximum.

G703 Speed: 1.5 ms at least security to 9.5 ms at greatest security.

VF Speed: Depending on qualifying time, security settings, frequencies and bandwidth set, operating times from 8 ms (360Hz shift, N = 1, M = 8, 0 ms qualifying time, 0.25 ms debounce) to 40 ms (60Hz shift, N = 1, M = 8, 0 ms qualifying time, 0.25 ms debounce).

Counters: Up to 8 counters of 3 digits to record trips sent and received.

Alarm/status Relays: 8 or 16 C/O relays rated at 2A @ 48 VDC, 300mA @ 300VDC. Any alarm or status condition can be directed to any relay including common alarm relay. Alarm sources may be ORed to any relay. Relay on-time delay can be set. Relay can be latching or self resetting.

G703 Communications: CCITT G703 64Kb/s, normal contra-directional operation and normal slave co-directional operation available for use with multiplexers. A master co-directional mode available for terminal to terminal operation and G703 loopback mode.

G703 Security: N valid frames out of M successive frames with N and M values from 1 to 16.

VF Communications: CCITT G232 based. Frequencies can set to higher frequencies than G232 requirements. Analogue loopback, digital loopback and normal modes.

VF Levels: Transmitter output range from -35dBm (single tone) to +3dBm (single tone).
Receiver input range is from -40dBm (single tone) to +10dBm (total energy).
Transmitter level accuracy is +/-1dB. Receiver level accuracy is +/-1.5dB at the guard frequency, mid channel levels may read 3dB higher depending on setup.

VF Frequencies: Any trip and guard frequency from 300Hz to 3825Hz in 15Hz steps can be used.
Available shift frequencies are 60, 90, 120, 150, 180, 240, 300 and 360Hz.
Frequency accuracy is +/-1Hz.

VF Received Noise: Dual discriminator on each FSK channel, each with trip, guard and noise outputs.
Inhibit activated when signal and white noise are of equal amplitude, +/-1.5dB.
Receiver operation suspends when signal is greater than 8dB below the noise level.

VF Loss of Guard: High speed LoG for detection line separation and high noise on PLC and other communication systems. LoG timing and security can be user set.

VF Security: Inhibit timers, command qualifying timers and channel correlation timers.
Receiver output options of "Inhibit to Guard", "Inhibit Alone" and "Hysteresis Bias".
N valid samples out of M successive samples with N and M values from 1 to 16.
The values of N and M also adjust the receiver discriminator output transition thresholds, in proportion to N divided by M. Dual or single FSK channel operation.

VF Boost Input: 40VDC to 180VDC, internal resistance of 10000 ohms.

Trip Timers: Trip input debounce, input extend time and output extend for each command channel. Cut off time and hold off time common to all.

Self test: All input/output and communication functions under continuous test.

Selectable Ranges:

'N'	1 to 'M'	
'M'	1 to 16	
Input extend	0 to 990 msec.	
Output extend	0 to 990 msec.	
Qualifying time	0 to 99 msec.	(VF only)
Inhibit onset time	0 to 99 msec	(VF only)
Inhibit extend time	0 to 99 msec	(VF only)
Correlation	0 to 200 msec	(VF only)
Hold off time	0 to 200 seconds	
Cut off time	0 to 200 seconds	
Debounce time	0 to 100 msec	

Refer section 1.2 (Security)

Withstand Voltage: Power supply, boost input, command input, command output, VF pilots and common alarm relay to 5000VDC. Other alarm relays to 2500VDC. G703 and LAN terminals to 500VDC.

Impulse at 0.5j: Power supply, boost input, command input, command output, VF pilots and common alarm relay to 5000V. Other alarm relays and LAN to 2500V. G703 terminals not rated for impulse.

Disturbance: Power supply, boost input, command input, command output, VF pilots and common alarm relay to IEC-255-22-1 Class 3. Other alarm relays to IEC-255-22-1 class 2. G703 and LAN terminals to IEC-255-22-1 class 1 (no test required).

Connections: All termination at rear on plug-in terminals suitable for 2.5 sq. mm cable.
Plug-in mating connector supplied.

Ambient Conditions: Designed to exceed IEC834-1. -5°C to +55°C

Physical Size: 19 inch 3 U high rack mounting. Depth. 355 mm.

Mounting: Flush or semi projection mounting.

Weight: 6.5Kg. approx. (depending on modules fitted.)

Shipping weight: 7.5Kg. (maximum)

SECTION 3

Installation.

This chapter contains instructions for the unpacking, mounting and the interconnection wiring of the Dewar DM1200 terminal

3.1 Unpacking.

Dewar DM1200 terminals are supplied as complete systems. All plug-in card modules are housed within the chassis.

1. Care should be taken when opening and removing the packing material from the carton.
2. Ensure that two brackets and four mounting bolts are included in the carton.
3. Remove the front panel and inspect the plug in modules are correctly housed within the chassis.
4. Inspect the rear of the chassis and ensure that all mating connectors are present
5. Missing material or shipping damage should be notified to Dewar customer service or your authorised Dewar agent immediately. All cartons and packing material should be kept if making a claim for damage with the shipping company.

3.2 Mechanical.

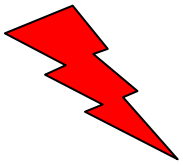
The terminal fits a standard 19-inch rack and occupies 3 rack units. The supplied reversible mounting brackets which bolt to the side panels permit flush or semi projection mounting of the terminal. Provision is made on the top of the terminal for the fixing of a "tally plate". Refer drawing 4-313-82. Terminal Dimensions.

***** WARNING *****

The 1/4 Whitworth bolts used to secure the mounting brackets and M4 bolts securing the tally plate must not protrude into the unit more than 7 mm. from the outside surface otherwise damage to internal components may result.

3.3 Terminal Connection Wiring.

The provision of Dewar supplied rear mating connectors makes for ease of installation. It is suggested to pre-wire the connectors prior to the mounting of the Dewar DM1200 terminal. Drawing 3-313-548 shows the designations of the terminals. Wire may be solid or stranded, up to 2.5sq. mm. The terminal layout is so arranged that the communications wiring (class II) and the command wiring (class III) may be loomed separately and fed from opposite sides of the terminal.



***** DANGER *****

Voltage potentials associated with the operation of this equipment can be lethal. Do not attempt any wiring connection until it has been ascertained that all power has been disconnected.

For terminal schematic refer to drawing 3-313-521

A basic description and connection of all terminals follow

TB1 to TB16. Alarm Relay Outputs

The terminal can be purchased with one or two alarm relay output cards. Each card contains eight relays with a single set of change over contacts. Depending on the alarm requirements each relay should be wired accordingly. At installation set up the relay cards fitted are monitored and warnings are given of any alarm selection is made to an unfitted relay card.

TB17. Monitor.

No connection. Not used.

TB18. Optional LAN Connection.

This allows for “local area network” communication between terminals

TB19. Power Supply, Boost Input, Common Alarm Relay.

Power Supply:	Battery input connection. (Irrespective of battery voltage used)
Boost Input:	Connect only if using boost control on the terminal being installed.
Command Alarm Relay:	Facilitates for two alarm outputs. Consists of two sets of changeover contacts

TB20. Expansion.

No connection. Not used

TB21. Processor

Digital Communication. (G703)
Pins TB21-1 to TB21-8 are only wired for digital connections

Co-Directional operation.
Pins TB21-1 to TB-4 only

Contra-Directional operation.
Pins TB21-5 to TB21-8 only

VF Communication. (Voice Frequency Tones)
TB21-9 to TB21-10 are only wired for VF “send” connection.

TB22. Processor.

TB22-1 to TB22-2 is only wired for VF “receive” connection.

TB23 to TB26. Trip I/O Command.

The trip I/O commands allow for the installation of up to two modules for VF and four for G703 applications, Modules are available in two nominal output voltage ranges, 240 volt and 120V.

Depending on the quantity of I/O cards used, placement should be in sequential order starting from I/O 1 through I/O 4 as identified on the inside front panel.

Inputs. Trip input command connections are labelled High, 240V. Mid 120V Low and -Com. Low covers 48V, 32V and 24V. Depending on the voltage of the trip input voltage being used the wiring connection should be made between the appropriate voltage level and -Com.

Outputs. Each trip facilitates up to three trip outputs signals via normally open relay contacts. If a trip occurs each of the three output relays are activated. At least one output must be connected and "A" is the recommended initial connection. All three output connections are polarity sensitive.

PL5. RS232.

The RS232 connection can be used to access remote DM1200 systems to configure or download history of events. The RS232 connection utilises a standard DCE 9 pin D female connector.

Earth 2 & Earth 3

Terminal earth. These earth points mate with 6.3 mm spade receptacles. It is suggested that the earth should be hard wired to the user's mounting rack.

For the self test of the output circuits to operate, a voltage must exist between the command output terminals. Should the **DEWAR DM1200** outputs be connected in series with other contacts, resistors can be used to maintain a voltage of at least 18V across the output. The value can be calculated from the command battery voltage and internal resistance of the output circuit which is 600K Ohms.

Where this procedure is not acceptable, a circuit may be programmed as **SIT** (series intertrip) to suppress a **Trip Output Fault** alarm when there is no voltage across the trip output terminals. This approach limits the ability of the self test system to report output faults.

When connecting the command outputs, the lower numbered command terminals should be used in preference, ie.. if one or two command output contacts are to be left unused on a trip IO card, it is the higher numbered terminals that should be left unused. The number of used contacts should be setup in the menu to stop the unconnected output contacts producing alarms.

The command input connections are arranged in three main voltage ranges. HIGH is 240 volt command input +wire, MID is for 120 volt command input +wire and LOW is for 24, 32 and 48 volt command input +wire (NOTE: The trip IO card has links also to select the LOW command input voltage range and enable the MID range). The COM is a common negative.

3.4 Voltage Selection. (Power Supply)

The power supply board must match the communications battery voltage in use. Power Supply board Model 1200-42 covers nominal voltages of 24V, to 48V. Model 1200-43 covers 110 to 320 V. The terminal is keyed to prevent a low voltage unit from being fitted to a terminal intended for a high voltage unit.

***** WARNING ***.**

Failure to select the correct voltage could result in either damage to a card or unreliable operation.

The nominal command input voltages are selected by a combination of terminal board connections and shunt links on the Trip I/O board. For 240, 120 or 48V inputs, the shunt should be fitted to LK3. Input is connected to -COM and +HIGH, +MID or +LOW as appropriate. For 24V, the shunt is fitted to LK1 or for 32V, to LK2. Input is connected to -COM and +LOW.

TRIP I/O

The TRIP I/O board is manufactured with high or low current output devices. The high current version (Model 1200-31) is restricted to 120V operation while the low current version (Model 1200-30) can be used at all voltages up to 240V. The terminal is keyed to prevent a low voltage unit from being fitted to a terminal intended for a high voltage unit.

3.5 Testing.

When installation is complete, the wiring should be tested. The **DEWAR DM1200** has features to facilitate testing. Reference should be made to sections 4 and 5 for the selection of these features.

3.5.1 Battery Supply.

To switch on, press the power switch in. The **RUNNING** light should glow. Select **PSU Voltages** from the **INFORMATION** menu and read the battery voltage. Note that this voltage is approximate only.

3.5.2 Trip Inputs.

Select **Watch Inputs** from the **OPERATIONS/Manual Trip Test** menu. The trip input status and counters will be displayed. The command input circuits can now be energised and their operation monitored.

3.5.3 Trip Outputs.

The command output circuits are tested by selecting 'Manual Test' from the operation menu.

3.5.4 Terminal to Terminal Test.

The terminals at both ends of the communications link should be set to the correct communications mode as described in section 4.4. Inspect the **Alarm Status** from the **INFORMATION** menu. There should be no current alarms indicated. Manual command tests as described in section 5.3 will verify the operation of the system.

3.5.5 In-Service Testing.

Once installed, the automatic self- test will detect almost all possible equipment and communication faults and loss of external supply to the output tripping devices. However confidence in the system integrity can be maintained by periodic manual testing. Manual tests, as described in section 5.3, can be carried out.

On the G703 terminal, a loopback mode may be used to check the local terminal. Since the local loopback mode is sent to the remote monitor, the remote monitor disables command processing at the remote monitor. The transmission of the loopback condition through the G703 supervisory link can take up to 12 seconds from the time the new setup is saved.

On the VF processor, using the internal loopback negates the necessity to set the local transmitters and local receivers to the same frequencies, bypassing the local receiver filters. If the VF supervisory link is enabled the loop back condition will be sent to the remote end, stopping the remote end receiving commands. The transmission of the loopback condition through the VF supervisory link can take 32 seconds and longer if trip activity is present, from the time the new set up is saved.

***** WARNING ***.**

When loopback testing the local terminal, failure to select loopback on the remote terminal may result in the reception of unwanted trips at the remote end.

The status of the remote terminal may be determined by selecting **Remote Status** from the **INFORMATION** menu.

3.5.6 Terminal Identity Check

The **DEWAR DM1200** provides a facility to give security against the possibility of cross connection of communications bearers by checking the source identity of received signals on the G703 and VF communications channels. If identity checking is enabled, the Operations Menu pass codes (see Section 4.3) of both terminals must match before command operation is enabled by the monitor modules. The major firmware version number (the number to the left of the point) should match for compatibility between processor and monitor modules on both the local DM1200 terminal and the remote DM1200 terminal.

SECTION 4

Setting Up.

4.1 Controls.

The controls on the **DEWAR DM1200** have been kept to a minimum. The Power Supply uses a push on-push off power switch. The LED below the switch glows when the power supply is operating.

The Monitor module provides the mechanism for setting up the terminal. Under software control, Liquid Crystal Display and a soft-touch keypad replace the need for setting of potentiometers, switches and most links.

The monitor LCD display backlight will flash to indicate that an event, either a command or an alarm, has occurred. Should the display remain dormant for a period of time, the screen will be blanked to conserve display life. Operation of the cursor or enter key will restore the display.

A push button on the Processor card, when used in conjunction with the manual test menu initiates the sending of a trip for test purposes.

There are shunt links on each of the Trip I/O cards for the selection of trip input voltage range.

Selecting “SET DEFAULTS” from Setup menu can make factory default settings for all firmware parameters. (For values refer Appendix B.)

Terminal set up menus can be set up in the field or in the workshop. Access to set up menus can be performed in a variety of ways.

4.1.1 Setup via Monitor Front Panel.

Information or menus are displayed on a 4 line x 20 character backlit LCD. The cursor keys, marked with four direction arrows, enable the display to be scrolled up or down or the cursor to be moved horizontally along a line. An enter key, indicated by a back arrow (enter), is used to accept the menu item indicated by the cursor. An escape key provides the facility to abort the current menu settings.

4.1.2 Setup via RS232.

Information and setup menus can be accessed through the RS232 port and to local terminals via the LAN. To setup an RS232 connection to a personal computer (PC), the DM1200 is connected to the PC's COM port. The DM1200TALK program is used on the PC to communicate with the DM1200 terminal. See Appendix D for more information on connecting to a PC.

Using the RS232 connections provides the same key functions as the Monitor front panel display. The RS232 connection also allows the use of all the keys on the PC, shortening the setup time. Information menus use the full screen.

RS232 connection allows setup HEX files to be sent to and dumped from the DM1200 terminal.

4.2 Menu Operation.

The menus are arranged in a hierarchical structure with the main menu at the top. The menu system allows the selection of all the setup and status displays. Menus are navigated by using the cursor keys. Place the cursor on an item and press enter. Selecting the "EXIT" menu item or pressing the escape key exits the current menu and retraces the hierarchical menus, one step back towards the main menu. When the main menu is reached, pressing the escape key again turns off the LCD display (ie. the same as selecting **FINISHED** in the **INFORMATION MENU**).

Upon entering a menu, the cursor will be positioned on the current setting. If a setting is changed, a confirmation message will be displayed briefly. The change will be effective immediately but on leaving the setup menu you will be asked whether or not you want to save the settings. If you press enter, these settings will continue to be used, otherwise the changed settings will be lost.

4.2.1 LCD Menu Operation.

With the limited display size, the menus are self explanatory. Once a menu has been selected, the menu title and level number are displayed on the top line, followed by a number of selections. Where the number of selections exceeds three, it is necessary to scroll to view all items.

Where input is required, this may be performed either by making a selection from a series of choices or by entering a number. Since there are no numeric keys, numbers are entered by incrementing or decrementing the displayed value using the up or down keys. The size of the increment or decrement may be changed by the left and right keys. The program will restrict values to sensible limits.

4.2.2 RS232 and LAN Menu Operation.

The menus display with RS232 and LAN operation allow full screen utilisation.

The keyboard also allows numbers to be entered directly. Once a menu has been selected, the menu heading level number is displayed on the top line, followed by a number of selections. The header line also indicates the presence of trip and alarm events, and the terminal's LAN ID number. The screen shows all available selections.

Where input is required, this may be performed either by making a selection from a series of choices or by entering a number. Numbers can be entered directly. The program will restrict values to sensible limits.

For details of the menu structure, refer to appendix A.

4.3 Access to Menus.

To restrict unauthorised tampering, passcodes can be setup to gain access to "SETUP", "OPERATIONS" and "MAINTENANCE" menus. If the passcode is set to "0000", access to the menu is unrestricted. If the passcode has been set to another value, you will be requested to enter a passcode. For further security a different passcode can apply to each menu.

4.4 G703 Communication Modes.

CO-DIRECTIONAL SLAVE	for a 4 wire connection through a multiplexer or direct to another terminal.
CONTRA-DIRECTIONAL	for an 8 wire connection through a multiplexer.
CO-DIRECTIONAL MASTER	for a 4 wire connection directly to another terminal programmed as co-directional slave.
LOOPBACK	used to test a single terminal. The trip inputs are not processed and the send signal is modified to prevent the remote terminal from responding to commands.

NOTE: All G703 modes pass supervisory data between the local and remote monitors. The G703 supervisory link may take 12 seconds to transfer the loopback status to the remote terminal

4.5 VF Communications Modes.

NORMAL	used as the normal two tone FSK transmitter to receiver operation between terminals. The supervisory link is turned off.
SUPERVISORY LINK ON	enables the uses of a four tone FSK principle for transmitter to receiver operation between terminals. The frequencies used pass the normal trip and guard states along with supervisory data for the local and remote monitor modules, see section 6.4 for more information.
LOOPBACK	used to test the transmitter and receiver on a single terminal. The receiver analogue input is connected to the transmitter's analogue output. The receiver automatically sets to the same frequencies as the transmitter to allow loopback operation. The trip inputs are processed and sent to the remote. The supervisory link is enabled. If the remote receiver has the supervisory link enabled, the remote monitor will stop trip processing on the remote VF processor and indicate the loopback status.
INTERNAL LOOPBACK	used in diagnostic testing on a local terminal to remove the analogue processing delays (eg group delays, comm's delay, etc) from the response time.. The loop back is done from the transmitter's digital output to the receiver's digital input internally. All timing functions are still active (eg qualifying time). The trip inputs are processed and sent to the remote also. The supervisory link is enabled. If the remote receiver has the supervisory link enabled, the remote monitor will stop trip processing on the remote VF processor and indicate the loopback status.

Note. The VF supervisory link may take 32 seconds to transfer the loopback status to the remote terminal.

4.6 Alarm Allocation.

Alarms and trips are all reported to the screen and these events may optionally be reported to alarm relays.

Code	Short Name	Comments
1	**RECD SIGNAL LOSS**	No receiver signal on G703.
2	**AIS CONDITION**	'Mux' has sent 'all ones' on G703.
3	**HIGH BIT ERROR**	Bit error rate high on G703.
4	**#1 INPUT FAULT**	Trip 1 input circuit failed.
5	**#2 INPUT FAULT**	Trip 2 input circuit failed.
6	**#3 INPUT FAULT**	Trip 3 input circuit failed.
7	**#4 INPUT FAULT**	Trip 4 input circuit failed.
8	**OUTPUT S/C FAULT**	Trip output has a short circuit.
9	**#1 OUT O/C FAULT**	Trip 1 output has an open circuit.
10	**#2 OUT O/C FAULT**	Trip 2 output has an open circuit.
11	**#3 OUT O/C FAULT**	Trip 3 output has an open circuit.
12	**#4 OUT O/C FAULT**	Trip 4 output has an open circuit.
13	**PSU WARNING**	Power supply voltage out of tolerance.
14	**#1 FORCED CUT-OFF**	Trip 1 terminated by time-out.
15	**#2 FORCED CUT-OFF**	Trip 2 terminated by time-out.
16	**#3 FORCED CUT-OFF**	Trip 3 terminated by time-out.
17	**#4 FORCED CUT-OFF**	Trip 4 terminated by time-out.
18	**#1 HOLD-OFF ALARM**	Another trip 1 occurred during hold off time.
19	**#2 HOLD-OFF ALARM**	Another trip 2 occurred during hold off time.
20	**#3 HOLD-OFF ALARM**	Another trip 3 occurred during hold off time.
21	**#4 HOLD-OFF ALARM**	Another trip 4 occurred during hold off time.
22	**REMOTE ALARM**	Remote Communications failure or alarm.
23	**MONITOR FAULT**	Monitor alarm, setup failures.
24	**PROCESSOR FAULT**	Teleprotection processor failure.
25	**OFF NORMAL**	Terminal "OFF NORMAL" (eg. setup, test, etc.).
26	**#1 SENT**	Trip 1 being sent, slow speed copy.
27	**#2 SENT**	Trip 2 being sent, slow speed copy.
28	**#3 SENT**	Trip 3 being sent, slow speed copy.
29	**#4 SENT**	Trip 4 being sent, slow speed copy.
30	**#1 RECD**	Trip 1 being received, slow speed copy.
31	**#2 RECD**	Trip 2 being received, slow speed copy.
32	**#3 RECD**	Trip 3 being received, slow speed copy.
33	**#4 RECD**	Trip 4 being received, slow speed copy.
34	**POWER FAIL**	Power failed (records on / off times of the power supply).
35	**IDENT FAIL**	Terminal to terminal Identity Alarm
36	**TRANSMITTER ALARM**	Transmitter fail (VF processor only).
37	**RECEIVER ALARM**	Receiver fail (VF processor only).
38	**INHIBIT ALARM**	Trip out inhibited (VF processor only).
39	**ACCESS**	Monitor access alarm.
40	**COMMON ALARM**	Common alarm.

Table 4.6 Alarm Event Sources

As the number of events exceeds the number of alarm relays, it is necessary to perform an allocation process whereby events can be directed to specific relays. The number of relays available depends upon the relay cards fitted. Information as to the number of relays is given in the INFORMATION menu. It is permissible to OR any number of events to the same relay or to leave sources un-allocated. As each event is selected, the following selections must be made:

Time delay before relay operates,
Relay number (provision is made to drive one relay or a relay pair),
On or off stated of the relay,
Latching (relay resets only when event is acknowledged) or non-latching,
Include or exclude the event from the common alarm relay action.

NOTE: LoG signal can be output from the alarms relays. log's output from trip IO 1 can be output to alarm relays as #3 RECD. log's output on trip IO 2 can be output to alarm relays as #4 RECD. This correlation only applies to the LoG to alarm relay connection. The LoG events are stored in the trip status as LoG# events.

4.7 Performance Setup.

The response time, security and dependability setup depends on the setting of a number of parameters.

To help speed up performance setup, each processor type has default settings to set application performance to a known starting point. Refer to Appendix B for the default parameters used. Table 4.7 shows typical applications used for each performance type.

Table 4.7 Performance Setup for Common Applications

Default Setting	Description	Typical Application
"HIGH SPEED"	High dependability, low security, high speed.	Blocking applications.
"OPTIMUM"	Medium dependability, security and speed.	Permissive tripping applications.
"HIGH SECURITY"	Low dependability, high security, slow speed.	Direct tripping or inter-tripping applications.

4.7.1 G703 Default Performance.

Table 4.7.1 G703 Processor Default Performance

Menu Selection	Description	Response Time at BER 1E-6 (mS)	Security at BER 1E-6 (Puc)	Dependability at BER 1E-6 (Pmc)
High Secur'Codir	High security co-directional slave.	4.5	0.0	0.0
Fast Resp' Codir	Fast response co-directional slave.	2.5	0.0	0.0
Optimum Codir	Optimum co-directional slave.	3.5	0.0	0.0
High Secur'Contra	High security contra-directional.	4.5	0.0	0.0
Fast Resp' Contra	Fast Response contra-directional.	2.5	0.0	0.0
Optimum Contra	Optimum contra-directional.	3.5	0.0	0.0

NOTE: A BER of 1E-6 (1 error bit in 15.6 seconds) has no effect on Puc (possibility of an unwanted command) and Pmc (possibility of a missed command) in the DM1200 terminals due to the line code. If a single error bit occurs every M * 32 bits, the output response by 1 frame (500 μS) if the error bit occurs at the transition from guard to trip.

4.7.2 VF Processor Default Performance.

Table 4.7.2 VF Processor Default Performance

Menu Selection	Description	Response Time at SNR 9dB (mS) typical	Security at SNR 0dB (Puc) Worst Case Noise	Dependability at SNR 9dB (Pmc)
Dual Ch HiSec'y	High security dual channel 240 Hz FSK.	21.3	< 1e-6	< 1e-3
Dual Ch Optim	Optimum dual channel 240 Hz FSK.	17	< 1e-4	< 1e-4
Dual Ch Fast	High speed dual channel 240 Hz FSK.	13.5	0.00095 typ'	< 1e-5
Single Ch HiSec'y	High security single channel 240 Hz FSK.	21.8	< 1e-6	< 1e-3
Single Ch Optim	Optimum single channel 240 Hz FSK.	17.9	< 1e-4	< 1e-4
Single Ch Fast	High speed single channel 240 Hz FSK.	14.7	0.0009 typ'	< 1e-5

VF Performance Notes.

With reference to table 4.7.2, the following must be considered with reguard to performance;-

1. An INHIBIT condition is detected when the 'in channel signal' (in mVrms) divided by the 'in channel noise' (in mVrms), SNR, is less than or equall to 6 dB (+/-1 dB). The INHIBIT condition forces the guard condition by default.
2. SNR values greater than 9dB have no effect on response time, Puc (possibility of an unwanted command) and Pmc (possibility of a missed command).
3. An SNR value of 6 dB will increase the response time by a factor of upto 2.
4. Varying SNR values will have no efect on Puc. The Puc performance is measured at 'worst case'.
5. At 6 dB SNR, the Pmc will start to increase. At an SNR of 0 dB the Pmc will be 1.0, and it will not be possible to receive a command.

4.8 Trip IO Timers.

There are five timer functions associated with each trip command:

Table 4.8 Trip IO Timers Purposes

Timer	Description	Purpose
Debounce	Provides a time period minimum during which the input trip command must be stable before the trip is accepted by the system. Specifying a value of zero will remove this function.	Prime purpose is to make system immune from input spikes but can also be used to delay transmission. A secondary purpose to adjust response time by delaying the trip transmissior
Input extend	Used to extend the trip sent. Specifying a value of zero will remove this function.	Provide a minimum trip transmission time in cases where trip input may be too short for adequate dependability.
Output extend	Used to extend the trip output. Specifying a value of zero will remove this function.	Provide a minimum trip output time when the received trip command is output equipment which requires a longer trip hold time.
Cut-off time	Forces the trip output to cut off if the trip during exceeds the cut-off time. Specifying a value of zero will remove this function.	To set a maximum time limit on the trip output is case where a continuous trip output may overheat, etc. connected equipment (ie limits t trip output duty cycle).
Hold-off time	Determines the minimum amount of time between two consecutive trip commands. Following the end of a trip output (normal or cut-off), a new trip output cannot be established until the expiration of the hold-off time. Specifying a value of zero will remove this function.	To set a minimum time period on the guard output (ie not trip state) to allow connected equipment time to recharge.

4.9 VF Log of Guard (LoG) Output.

The VF receivers can detect the absence of a guard tone or a trip tone in the FSK channel. The speed of detection and output is controlled by the inhibit onset timer setting on each VF receiver channel. If dual channel receiver operation is used, both receivers must detect LoG to allow the output of the LoG signal from a second trip IO module.

4.10 Automatic Detection Setup.

The DM1200 terminals can be quickly setup by selecting "SET DEFAULTS" from the "SETUP MENU", and then selecting "AUTODETECT". The monitor module will find the processor type, the trip IOs fitted and the trip outputs circuits used. The monitor will then ask for the appropriate performance defaults for the teleprotection application. The alarm relays are set to a standard factory default configuration applicable to the relay cards fitted.

The default settings can be used as a starting point for further setup changes (if required) or left to operate with the default settings. The new settings need to be saved.

The DM1200 terminal is shipped with the high security default applicable to the cards and modules fitted to the terminal.

4.11 Testing.

When the terminal setup is complete, the installation and setup will need to be checked. The DM1200 has features to facilitate testing.

4.11.1 Supply Voltage.

To switch on, press the power switch in. The RUNNING light should glow. Select PSU Voltages from the INFORMATION menu and read the battery voltage. NOTE: This voltage reading is approximate only.

4.11.2 Communications Test.

The terminals at both ends of the communications link should be set to the correct communications mode. Inspect the Alarm Status from the INFORMATION menu. There should be no current alarms indicated.

4.11.3 Trip Inputs.

Select Watch Inputs from the OPERATIONS / Manual Trip Test menu. The trip input status and counters will be displayed. The command input circuits can now be energised and their operation monitored.

4.11.4 Trip Outputs.

The command output circuits are tested by selecting Manual Trip Test from the OPERATIONS menu. The Manual Trip Test procedure requires that both DM1200 terminals are installed are running. Manual command tests as described in section 5.3 will verify the operation of the system..

4.11.5 In-Service Testing.

Once installed and setup, the automatic self- test will detect almost all possible equipment and communication faults and loss of external supply to the command output circuits. However confidence in the system integrity can be maintained by periodic manual testing. Manual tests, as described in the user manual, can be carried out.

On the G703 and RS422 terminal, a loopback mode may be used to check the local terminal. Since the local loopback mode is sent to the remote monitor, the remote processor disables command processing at the remote end.

On the VF processor, using the internal loopback negates the necessity to set the local transmitters and local receivers to the same frequencies, bypassing the local receiver filters. If the VF supervisory link is enabled the loop back condition will be sent to the remote end, stopping the remote end receiving commands. The transmission of the loopback condition through the VF supervisory link can take 32 seconds and longer if trip activity is present, from the time the new set up is saved.

***** WARNING ***.**

When loopback testing the local terminal, failure to isolate the command output circuits on both ends may result in the reception of unwanted trips.

The status of the remote terminal may be determined by selecting Remote Status from the INFORMATION menu.

4.11.6 Terminal Identity Check

The DM1200 provides a facility to give security against the possibility of cross connection of communications bearers by checking the source identity of received signals on the communications channels. If identity checking is enabled, the identity number is Operations Menu pass codes on V6.00 or it can be programmed separately on V6.02 or higher. The identity number of both terminals must match before command operation is enabled by the monitor modules. The major firmware version number (the number to the left of the point) should match for compatibility between processor and monitor modules on both the local DM1200 terminal and the remote DM1200 terminal.

SECTION 5

Operation.

When setup (section 4) has been completed the terminal can be placed in service. The Information and Operation menus can be used to supervise the terminal operation.

5.1 LCD Adjustment.

The brightness of the LCD backlight and the optimum vertical viewing angle can be adjusted to suit the location of the terminal by Set LCD in the Information menu.

5.2 Events.

An event in this context refers to trip, LoG or alarm activity. The flashing of the display back lighting indicates that a change of the alarm or trip status has taken place. Selection of Trip Status or Alarm Status from the Information menu will identify the event. To acknowledge the event, press enter. When all events have been acknowledged, the flashing will stop.

An event log of past events is maintained and can be accessed from the **"Trip Status** or **Alarm Status"** menus. In the short form presentation four events are displayed at a time on the LCD, indicating event code and time only. A list of the event codes is given in Table 4.6. The left or right arrows permit toggling between this and a more detailed presentation.

5.3 Manual Test.

To perform a manual trip, select the Operations menu and select **"Manual Trip Test"**. Three modes of trip test are provided **Watch Inputs**, **Live Test** and **Safe Test**. Safe testing inhibits the trip outputs while live testing will generate trip outputs.

When the selection has been made, the terminal checks the status of the remote terminal. Unless the remote terminal has also had the same selection made, no test is permitted and a message is displayed.

When both terminals correspond, the desired trip number is selected. The **TEST** button is then enabled and the trip counters displayed. Pressing the test button will initiate a trip output at the remote terminal.

A manual test may be performed with a terminal in loopback, in which case the terminal performs as both local and remote terminals.

Selecting **Watch Inputs** enables the trip inputs to be observed on the display without being sent to the remote terminal.

5.4 Time-out.

To ensure that a terminal cannot be inadvertently left in **"Setup"** or **"Operations"** menus, after a period of no operator activity, the Monitor will ignore any changed setting and revert to the run mode, shutting down the LCD.

5.5 Off Normal.

An off normal condition exists whenever an operator has placed the terminal in a mode where normal operation is inhibited. The selection of Setup, Operations or Maintenance menus or the selection of Loopback communications mode results in an off normal condition.

Off normal is logged and can be directed to a relay, however it is not reported on screen as an alarm since it is the result of an operator action.

5.6 Access.

An access alarm is generated whenever a menu is active on the DM1200 terminal. The alarm ceases when **FINISHED** is selected.

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SECTION 6

Principles of Operation.

6.1 Overview.

The Processor controls the flow of data from the Trip input signal, through the bearer to the trip output. The Trip I/O cards provide the high voltage barrier between the field wiring and the Processor logic levels.

Two additional high voltage isolated sections are provided on the power supply card, output for a common alarm and input for VF transmitter boost.

The processor communicates with the Monitor module, also containing a microprocessor, which handles all the setup and supervisory functions. Once the operating parameters have been passed to the processor, the processing of trips proceeds without the intervention of the Monitor.

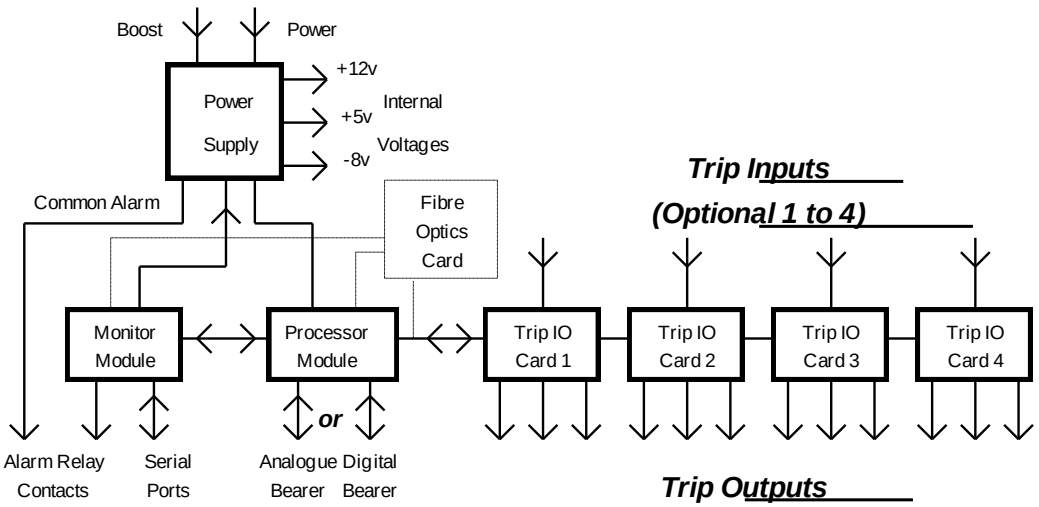

Fig. 6.1 Block Diagram of Terminal.

6.1.1 Processor / Monitor Interface.

The 5 lines that perform the communication between the processor and Monitor are: -

MON INTER: High level from Monitor to inform the Processor that the Monitor is present and operating.

DSP CLK: Data clock generated by the Processor.

FRAME SYNC: Pulse every 32 data clock cycles generated by the Processor to indicate the boundary between data blocks.

DSP OUT: Data from Processor to Monitor.

DSP DIN: Data from Monitor to Processor.

The data transferred to and from the Monitor is of two types:

1. Local data for setup tables, status and alarms.
2. Remote data for supervisory communications between monitor modules.

The **"local"** data is transferred in blocks of 4 bytes, each bit transfer occurring during DSP CLK high. The **"remote"** data flows through the processor to the remote terminal during DSP CLK low.

The local data to the Processor consists of the operating parameters as set by the user. The local data to the Monitor consists of trips sent and received, status and primary communications alarms.

The remote data facility provides a supervisory channel between the teleprotection terminals.

6.1.2 Processor - Trip I/O Interface.

To comply with the concept of immunity to tripping as a result of any one component failure, dual paths are provided throughout the **DEWAR DM1200** system. These paths commence at the trip input, follow through the Processor hardware and software, through the communication protocol and terminate at the trip output (refer also to Trip I/O section).

The signals in dual paths are referred to a **"Trip"** and **"Guard"**. A command is signified by the **"trip"** being asserted while the **"guard"** is not asserted. When no command is present, the assertion reverses. Additional signals are used during self -testing. Self -testing takes place continuously when no trips are being processed. The trip input path is tested by injecting a test current into the input. On the first test the current value less is than the threshold value and on the second test the value is above the threshold. The processor checks the responses from all trip I/O cards.

The output path is tested in three steps using the **"discrepancy"** signals to indicate the state of the transistor switches. In the first test, the guard and trip signals are such that neither switch is on, then the switches are turned on one at a time. At each step the processor checks the discrepancy signals.

6.1.3 G703 Command Input Processing.

The G703 trip and guard input processing is shown in figure 6.1.3.

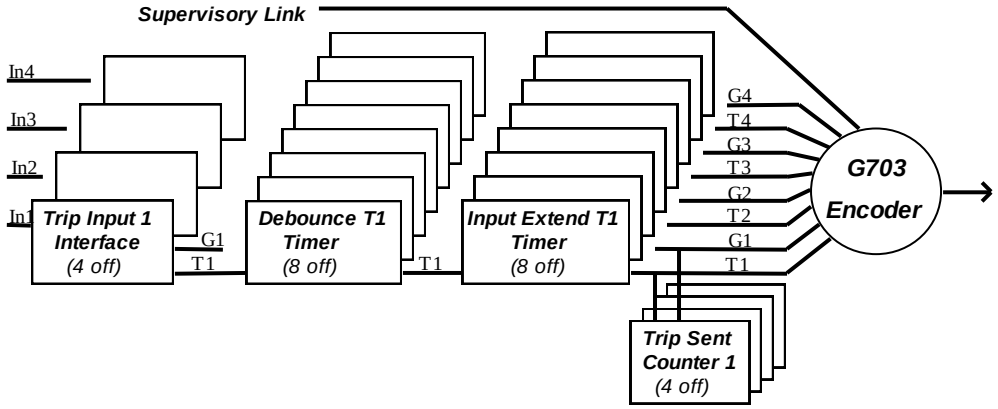

Figure 6.1.3 G703 Input Processing.

6.1.4 G703 Command Output Processing.

The G703 trip and guard output processing is shown in figure 6.1.4.

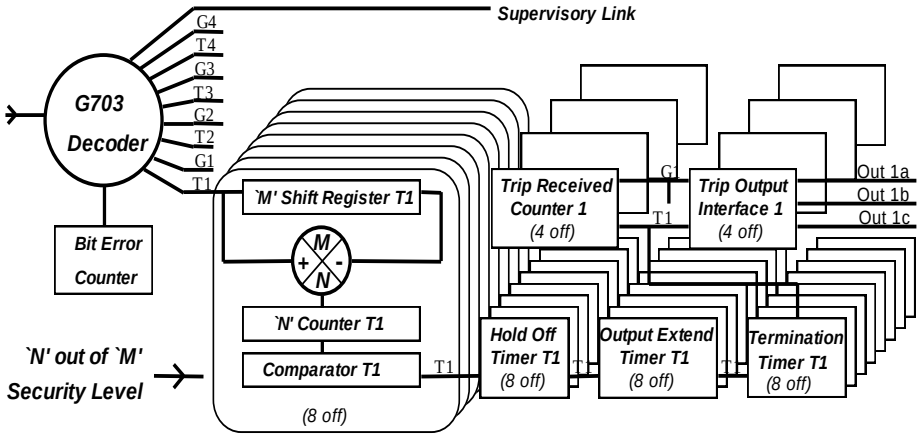

Figure 6.1.4 G703 Output Processing.

6.1.5 G703 Security.

The **DEWAR DM1200 provides** protection against the possibility of a false trip as a result of-.

1. Failure of a component
2. False activation of logic due to interference
3. Corruption of the transmitted code
4. Unauthorised or accidental manual testing.

1. The dual path philosophy ensures that no single component can result in a false trip. The failure of a single component, while not in itself capable of causing a trip, does leave the system exposed to the occurrence of a second fault which could do so. To remove this risk, a self test strategy is adopted where all components capable of causing a trip are subject to an automatic test sequence allowing the equipment to be taken out of service before a second fault occurs.

2. The form of construction ensures that the logic is well isolated from noise sources. The use of complimentary logic levels for the dual paths also assists in noise immunity. Independent processing of the paths within the processor software provides protection from memory corruption or program failure. The drive to the Trip I/O cards is inhibited if the processor stops running.

3. Corruption of the transmitted code is detected. The command is transmitted as a 32 bit sequence. This sequence is handled by the G703 interface as four 8 bit bytes (octets). Each byte contains three data bits, three check bits, one bit that is either a fixed one or used for other purposes and one bit which is used for byte identification.

The check bits are generated in accordance with a Hamming code that is capable of detecting all one and two bit errors and a high proportion of higher order errors. To further enhance the security a data count strategy is used. Each of the trip signals and guard signals has an associated register, the length of which may be adjusted up to 16 bits. This provides a window of length M of past data. When a valid data 1 is received, a 1 is shifted into the register. When a valid data 0 or an invalid sequence is encountered a 0 is shifted in. When the number of data 1s in the register equals or exceeds a value N, the data is validated. This validation is performed independently for the Trip and Guard paths.

The Hamming code is very effective in detecting random errors, however, because of the static nature of the trip and guard, data bits, the code could fail to detect certain systematic errors such as might be caused by sync slip in the bearer channel.

With static error patterns and static data the above N of M strategy is of no help. To overcome this problem a 4 bit sequence count is added. This breaks the stationary nature of the data sequence allowing the N out of M strategy to operate. In addition, the receiving terminal anticipates each sequence count and invalidates the data sequence if the received count does not match. The sequence recovery will require a further error free frame before a frame sequence can be validated. This provides a continuously interlocking line code.

Only when all 31 bits (supervisory bit is not checked by the processor) are free from detected errors and the sequence matches, is the 32 bit sequence validated.

These measures ensure that the probability of corrupted data being mistaken for a valid trip is very low. With N = 1, the possibility of generating a false trip from a random digital sequence is approximately 1 frame in 5.5E11 (8^13 frames, approximately 9 years).

6.1.6 VF Command Input Processing.

The VF trip and guard input processing is shown in figure 6.1.6.

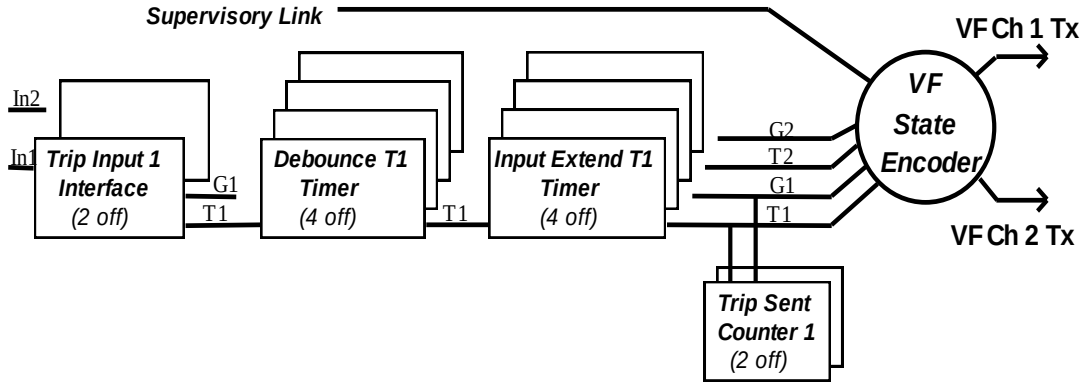

Figure 6.1.6 VF Input Processing.

6.1.7 VF Command Output Processing.

The VF trip and guard output processing is shown in figure 6.1.7.

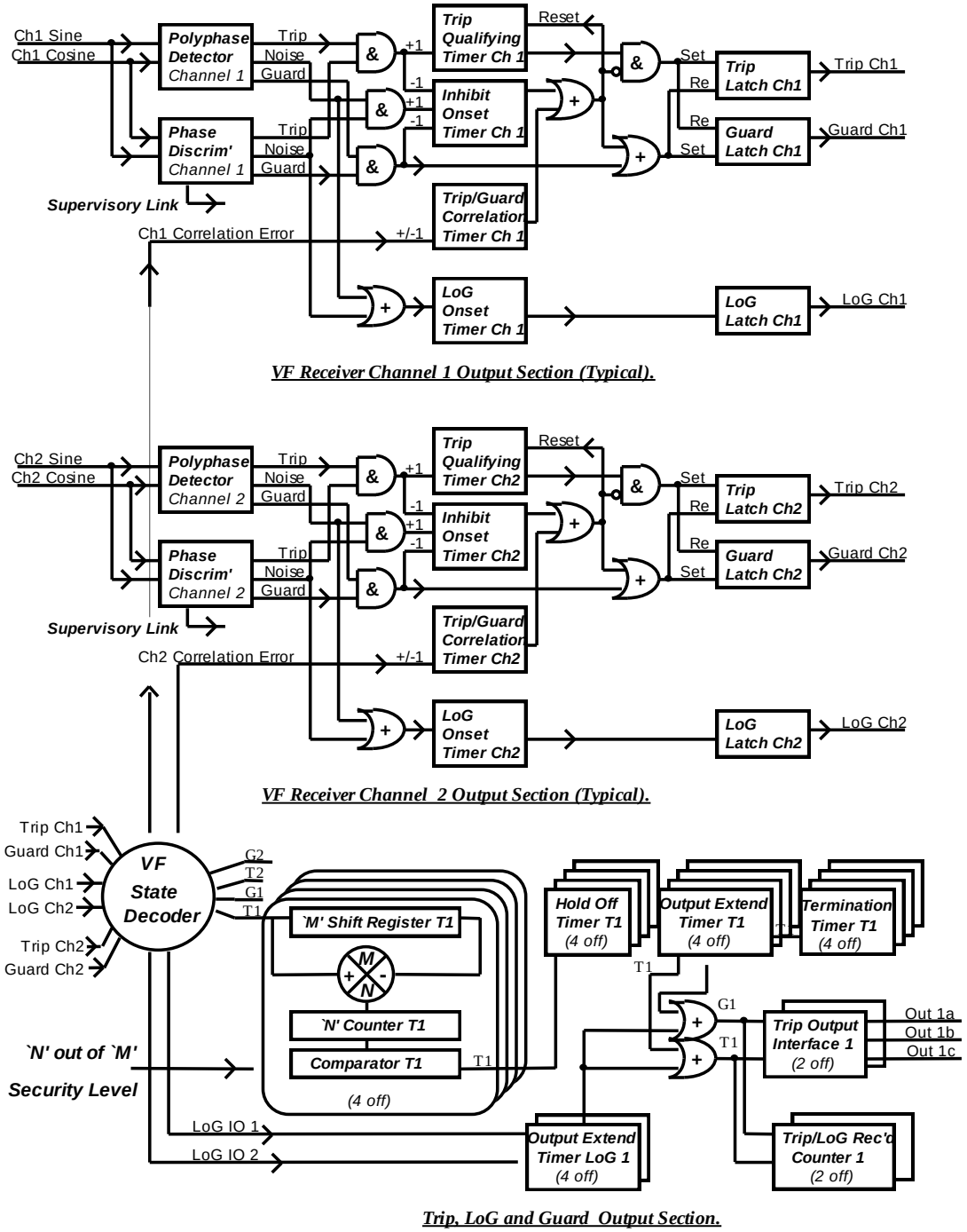

Figure 6.1.7 VF Output Processing.

6.1.8 VF Loss of Guard (LoG) Output.

The purpose of the LoG output is to signal external equipment that the VF channel tone has been lost. This is designed to pick arcing on a PLC line, when the high voltage wiring breaks carrying the PLC signals. The Log output responds to the 5 to 10mS of high level noise produced by the arc establishing across the break in the conductor. After the arc has established, the noise level drops, allowing the trip signal to be received by signalling through the arc. A second IO card (the same as a trip IO card) is used to output the LoG signal.

The LoG output signal is not present when trip or guard tones are present within receiver alarm level settings. If an LoG signal is required when a trip is present, an output contact on the LoG IO card can be paralleled with an output contact on the trip IO card.

The LoG output on each receiver, uses the noise detection outputs from polyphase and phase discriminators, the receiver level compared to the receiver minimum and maximum alarm point settings, and the receiver overload signal.

On a dual channel system both LoG1 and LoG2 must be active to allow the LoG output.

The LoG output events are recorded in the trip event log (as an LoG) and the trip IO card counter associated with the LoG output is incremented.

6.1.9 VF Security.

Security in a VF terminal is adjusted by the settings of N, M, Qualifying time, inhibit onset time, receiver options and the use of single or dual channel operation. The VF security relies on the noise detection processes in the receiver discriminators. The DM1200VF receivers each have two different discriminators, which both output trip, guard or noise. The two sets of outputs are logically analysed to provide the channel command state.

Receiver inhibit occurs when either of the discriminators detect noise for a user set inhibit time. The inhibit provides an alarm output to the monitor module and can be setup to force the guard command state.

With zero qualifying time and N = 1, the terminal responds to command change as fast as possible, but is vulnerable to false operation from noise.

An optimum setting for qualifying time, to balance speed against security, is 500 divided by the shift frequency, (eg. on a 240 hertz shift 2 ms qualifying is optimal). For optimal operation the inhibit onset timer should be set to 1000 divided by the shift frequency (eg. on a 240 hertz shift 4 ms inhibit onset is optimal).

High security settings for qualifying time start at 1000 divided by the shift frequency, (eg. on a 240 hertz shift, 4 ms). The inhibit timer should be set between half to three quarters of the qualifying time (eg. 2 to 3 milliseconds).

The value N and M work the same as in the G703 security, but with one added feature. Since the VF receiver is capable of discerning a 5 percent frequency change in the channel shift, the offset basis on the receiver discriminators can be adjusted by the ratio N divided by M. An offset of 1/3 (the lower limit) allows the output to change to the trip state when the channel frequency is one third from channel centre on the desired trip frequency side of centre. N / M = 1 ratios (eg. N=M) are not recommended when short response times are required, but this setting will increase security markedly.

On dual channel system (two complimentary FSK channels used for one command) the security is improved. The dual channel, operation can make use of the correlation timer to detect incorrect states of the two FSK channels. The setting of the correlation timers will depend on the difference in frequencies of the two FSK channels and the channel group delays in VF bearer used. A minimum of 1000 divided by the lowest shift frequency in use is recommended, typically correlation is set to twice the minimum.

However it is still possible for a random source to appear as a true trip signal on the input to the receiver, but the possibility of false trips can be greatly reduced by setting longer qualifying times and higher values for N.

The DM1200VF receivers can be setup to a hysteresis basis in their operation. In this mode the ‘inhibit’ does not force the guard command state. The received signal must satisfy the trip qualifying time and the N/M discriminator offset to change to the trip command state. Once in the trip state, the received signal must satisfy the guard qualifying time and N / M discriminator offset (on the guard side of the FSK channel) to return to guard command state. This provides trip and guard security by having the fail-safe condition of the last received state, stopping noise dropping the trip command state back to guard.

6.2 Monitor Module.

The monitor module is a multipurpose assembly based on a Z181 microprocessor. The monitor module consists of 3 main sections, microcomputer Card, front panel assembly and alarm relay cards.

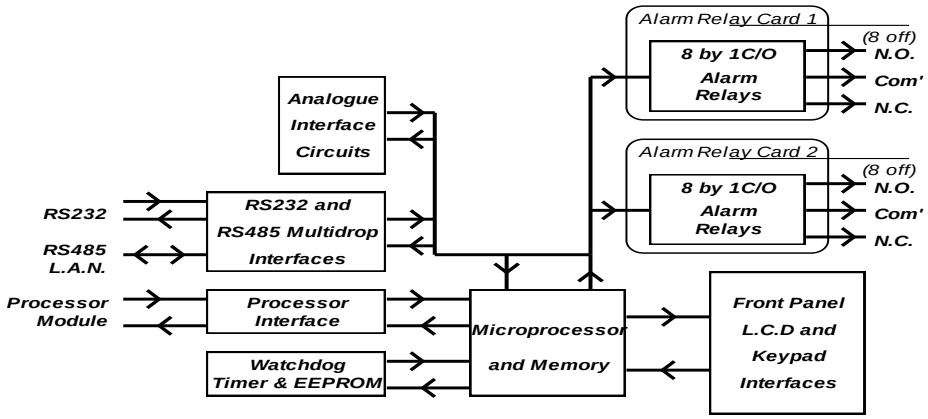

Fig 6.2 Monitor Module Block Diagram.

6.2.1 Monitor Microcomputer Card Assembly.

(refer to schematic diagram 3-313-125 items 1 and 2.)

The microcomputer Card has thirteen subsections to provide data interfaces and calendar information to the firmware in EPROM.

6.2.1.1 Microprocessor.

The microprocessor, IC12, is a Z181 intelligent peripheral controller. This device is an enhanced 10MHz Z80 central processing unit (CPU) plus most of the input/output structures for interfacing the firmware to the CPU. This includes two direct memory access controllers, two asynchronous serial receiver/transmitters, parallel input/output, a 1 megabyte memory manager, a clocked synchronous serial data channel and a high level serial communications controller. Various other elements are present but do not present signals outside the Z181.

The frequency of the 18.432 MHz crystal, XTAL1, is divided by two within IC12 to provide all timing references.

6.2.1.2 Monitor / Processor Interface.

IC12 communicates with the processor card is via IC24 for input and IC23 for output. The data is in synchronous serial form.

Signal inputs :-

DSP DOUT	serial data from processor card,
DSP DCLK	serial data clock from processor card,
FRAME SYNC	indicates start of the data frame,
FO SIG 1	expansion signal 1 from processor card,
FO SIG 3	async' data from VF processor card,
FO SIG 5	async' clock from VF processor card,
MON RESET	soft reset from processor card,
DSP INTER	firmware interlock from processor card.

Signal outputs :-

DSP DIN	serial data from monitor to processor card,
DSP DTOG	processor communication interrupt level toggle,
W/D TOG	watch dog timer toggle,
FO SIG 2	expansion signal 2 to processor and expansion cards,
FO SIG 4	async' clock to VF processor and expansion cards,
FO SIG 6	async' data to VF processor and expansion cards,
DSP RESET	hard reset to processor card,
MON INTER	firmware interlock to processor card.

Note that not all signals are used in this version.

6.2.1.3 Real Time Clock (RTC).

IC13 is a clock, calendar and RAM device. XTAL 2 provides the time reference for the RTC. CV1 is used to calibrate XTAL 2 by monitoring TP1 (TP0V return) for a 8192 hertz square wave. The RTC is battery backed via IC5. Two backup battery types can be used. Links LK1 and LK2 provide selection between the two batteries. Both links are open to preserve backup battery charge during storage. B1 is selected by LK1. B1 is not fitted by the factory. B1 is the same lithium battery as supplied on the 1200-10. B2 is selected by LK2. B2 is a 100mAH 3 volt rechargeable

lithium / vanadium battery. R20, R17 and D1 form a charger circuit for B2. The charger can recharge B2 in two days, from the 5 volt supply .

The RTC RAM is used to hold dynamic alarm data check codes.

The RTC is checked periodically for erroneous information. If an error is found a **"MONITOR ALARM"** is initiated.

6.2.1.4 Analogue to Digital Converter (ADC).

IC2 is an ADC1038 10 bit analogue to digital converter with serial interface. It contains the analogue multiplexers and the sample/hold. The analogue levels are input to IC2 from scaling networks associated with each input. IC1 provides a voltage reference of approximately 4.05 volts for IC2. The power supply to the ADC by filtered by R12, C3 and C6. Analogue address and control information, on TXS, is temporarily placed in IC9's shift register, as analogue data is read from the ADC, via RXS, the next analogue address is clocked, via CKS, into the ADC via the Z181's clocked serial IO port.

The ADC is used to monitor internal terminal supply voltage levels and where applicable, signal levels. Calibration is performed via firmware and stored in EEPROM.

6.2.1.5 Non-volatile Memory (EEPROM).

IC4 is a 4096 bit Electrically Erasable Programmable Read Only Memory (EEPROM) which requires no power to retain it's internal data.

IC4 holds user settings, calibration data, trip counters and firmware codes. EEPROM data is protected by check sums. The monitor periodically tests the check sum results. If an error is detected a **"MONITOR ALARM"** is initiated.

6.2.1.6 Firmware Memory (EPROM).

IC14 is a 512Kb by 8 bit EPROM. IC14 contains all the operating programs for the monitor module. This is called firmware as it resides in read only memory and requires the EPROM changes to be updated.

The content of IC14 is protected by a check sum. The monitor periodically tests the check sum result. If an error is found a **"MONITOR FAIL"** is initiated.

6.2.1.7 Random Access Memory (RAM).

IC16 is a 128kb by 8 bit random access memory (RAM). The RAM is used in two dynamically allocated sections, firstly for the dynamic firmware data and the remaining RAM is used for logging terminal events. The RAM is battery backed from RTC, IC13, backup supply. This preserves the alarm and trip logs during power failures. The firmware control table in RAM are reloaded, from the RTC, EEPROM and EPROM, on each pass through the firmware's main loop.

At power-on the RAM is tested. If the firmware finds it cannot obtain sufficient good RAM to run, the firmware must abort operation. If this happens, all monitor based alarms will be active and a continuous beep will sound but the state of the display will be undefined.

6.2.1.8 Liquid Crystal Display (LCD) Interface.

The LCD interface uses IC12's parallel IO signals P10 to P17 for data and P20 to P25 for control signals. The firmware initiates the slow control timing for the LCD via the SLOW IO DECODER, IC8. The IO signals connected to IC12 are damped by resistor networks RN1 and RN2. These provide surge current limiting on the interface signals.

6.2.1.9 Front Panel and Relay Card Interface.

The interface to the front panel assembly and the relay cards is via IC12's clocked serial IO port. Latching strobes are provided by IC8 which is controlled by P20 to P25.

Included in this interface are extra IO bits used for monitor control and testing.

Signal Inputs:-

TESTI0:	used in factory testing,
TESTI1:	used in factory testing,
LOW VCC:	is 0 level when IC5 detects the +5volt supply is low,
BOOST:	is 0 level when boost input to PSU card is active,
COM ALARM:	is 0 level when common alarm is active,
RELAY1INTER:	is 0 level when relay card 1 is present,
RELAY2INTER:	is 0 level when relay card 2 is present,
PANELINTER:	is 0 level when front panel Card is present.

Signal Outputs:-

TESTO0: used in factory testing,
TESTO1: used in factory testing,
Bit 7: is a common alarm inhibit.

6.2.1.10 Watch Dog Timer.

IC5, MAX690, is a microprocessor supervisory device. At power on IC5 provides the reset for the monitor module. If the W/D TOG signal does not change state within a predetermined time, IC5 will initiate another reset.

If the +5 volt supply falls, IC5 will pull the LOW VCC signal to 0 level stopping the RTC and the RAM from being disturbed. This signal is also used to stop the EEPROM being written during power outages.

6.2.1.11 RS232 Interface.

The asynchronous serial interface is provided by IC12, IC22, TR3 and associated components. A 9 pin "D" type female connector on the terminal board provides access to the terminal.

The RS232 provides the user with access to data from the terminal. If the terminal is networked, the RS232 connection provides the user with access to the data on all terminals.

The RS232 interface senses the presence of a completed RS232 connection via the RS232 DSR input signal. When this signal is inactive (-ve or open circuit) the RS232 interface is not used by the firmware.

It is expected that the monitor communications protocol will be tailored to the user requirement. Unless otherwise specified, the RS 232 port will mimic the messages sent to the screen and accept commands in the form of four arrow keys and **"ENTER"** on a PC keyboard. The "ESC" and numeric keys can be used and the menus are expanded to show more information. The RS232 interface is configured for 4800baud, 8 data bits, even parity, 2 stop bits.

6.2.1.12 Local Area Network (LAN) Interface.

This provides inter-terminal communication for logging and setup. The operation of the LAN allows a single terminal, connected to a host via a RS232, to access the monitor modules of other terminals on the LAN.

The high level serial communications controller in IC12 is used to provide protocol and timing functions implementing a high speed (50 kilobaud) interface between terminals requiring only a 2 wire twisted pair cable to each terminal. Each terminal LAN terminals are connected in parallel with the ends of the line terminated by 120 ohm half watt resistors (provided by the user).

As transmission and reception take place on the same terminal, IC11 provides co-incidence detection to stop collision of data packets. Co-incidence of transmissions is reported back to the originating firmware by the CTS signal and the line driver in IC21 is disabled. IC21 is a RS485 transceiver device. This device has the required driver output levels and receiver hysteresis to operate the single twisted pair user cables. T1 provides the electrical isolation between internal and external voltages.

The data is sent in packets that are checked for errors and re-transmitted if necessary to provide error free reception. Turning any terminal off does not effect the operation on the other connected terminals.

The length of twisted pair cabling is limited. The actual limit theoretically is 1 kilometre for only two terminals connected together. As a maximum of 20 terminals may share the same twisted pair, a recommendation of a maximum of 50 metres of cable be used.

6.2.2 Front Panel Assembly.

(refer to schematic diagram 3-313-122.)

The front panel assembly provides the mechanical fixation for the liquid crystal display module, front panel switches and the electrical connectors to relay cards. The front panel assembly has 4 subsections.

6.2.2.1 LCD Module.

The LCD module provides a visual character display of monitor menus, terminal settings, terminal levels and events. The display is 20 characters wide by 4 lines high.

When the display is not in use, the firmware turns the LCD off to preserve the display life.

6.2.2.2 LCD Viewing Angle.

To enable the LCD to be read at angles appropriate to its installation, the user can adjust the angle control voltage via the monitor firmware.

The viewing angle is output by the firmware to the five most significant bits on IC1. The five binary outputs are

converted to a voltage level by RN1: A, RN2, R2 and R9. This voltage is applied to the viewing angle control pin of the LCD. The viewing angle is adjusted over 120 degrees in 32 binary steps.

6.2.2.3 LCD Backlighting.

The LCD has LED Backlighting to allow the display to be viewed in low light levels. The level of backlighting is user adjustable in 8 steps. The firmware outputs the backlighting level to IC1 on the least significant 3 bits. R8, RN1:B, R7, D1 and R5 provide a reference voltage to the base of TR1. The collector current of TR1 is amplified by TR2. TR2's collector supplies the LED backlighting current to the LCD module. The LED return current is passed through R3. The circuit of TR2, TR1 and R3 provide a constant current source controlled by the voltage at the base of TR1. When alarms or trips occur, the firmware flashes the back lighting by alternating between the user set level and half the user set level.

6.2.2.4 Front Panel Keys.

The front panel membrane switch keys provide user input to the firmware. The keys are scanned by selecting the switch row (PD0 or PD1 high) and reading the switch closures via IC2.

6.2.3 Relay Output Cards.

(refer to schematic diagram 3-313-123.)

The terminal can be fitted with one or two relay output cards each equipped with eight relays with a single set of change over contacts. The relay card configuration is sensed by the monitor module assembly. The user is warned of alarm selections made to un-fitted relays.

The relay data is output from the firmware via the front panel card. The data is transferred to the output latch in IC1 by a strobe from the microcomputer card. The output of the latch is buffered by open collector drivers in IC2 to drive the relays. The clamping diodes for the relays coils are also contained in IC2.

Relay output card 1 contains relay functions 1 to 8 and relay card 2 contains relay functions 9 to 16.

6.2.4 Monitor Functions.

The primary functions of the monitor are:-

1. Provide most terminal setup facilities,
2. Send setup information to the processor,
3. Receive command and alarm information from the processor,
4. Update command sent and command received counters,
5. Monitor terminal operation,
6. Operate alarm output relays,
7. Log command and alarm events,
8. Maintain a data link to remote terminal's monitor,
9. Display terminal events,
10. Provide access for data logging devices,
11. Provide testing facilities.

6.2.4.1 Terminal Setup Facilities.

Internal functions to the terminal are setup via menu selections. Due to the LCD size all information, setup and testing operations have been broken down into small menus or information blocks suitable for display on the LCD. The displayed information can be stepped through by using the four cursor switches or a selection made by pressing the enter switch. See section 4.2.

The monitor is not able to setup the trip input or power supply voltage. This is hardware dependent and is dealt with in section 3.3.

6.2.4.2 Sending Command Setup to Processor.

The firmware sends setup information continually to the processor card via the processor interface. The transfer is under the control of the processor card.

6.2.4.3 Command and Alarm Information.

The firmware receives command and alarm information from the processor card continually. The alarm information is concerned with command irregularities, trip IO card failures and command communication failures. The transfer is under the control of the processor card.

6.2.4.4 Updating Command Counters.

The four trip received and four trip sent command counters are incremented by the monitor firmware. The command information passed from the processor card is interpreted to extract the leading edges of command events to increment the appropriate firmware counter. The counter values are stored in EEPROM.

6.2.4.5 Alarm Information.

During operation, the monitor firmware checks the following:-

1. terminal voltage levels (power supply WARNING alarm),
2. processor card operation (processor fail alarm),
3. validity of time and date (monitor fail alarm),
4. error free setup values (monitor fail alarm),
5. EEPROM checksum (monitor fail alarm),
6. EPROM checksum (monitor fail alarm),
7. remote alarms (from the monitor at the remote location),
8. stack irregularities (corrected but no alarm generated),
9. data overflows (corrected but no alarm generated).

6.2.4.6 Operation of Alarm Output Relays.

The firmware operates the alarm output relays according to the user specified destination for alarm signalling.

6.2.4.7 Log of Command and Alarm Events.

When any alarm or command event occurs, the firmware time and date stamps each occurrence. This log information is stored in the monitor's RAM.

Event check codes are stored in RAM for each event log. The check codes allow detection of corrupted log data. If corrupted logs are found, the corrupted event is displayed with a '$' character.

6.2.4.8 Supervisory Data Link to Remote Monitor.

The firmware maintains a slow speed serial link with the remote monitor. The purpose of this link is to communicate alarm conditions, terminal status and acknowledge manual testing of the command channels.

The remote link is via the processor card and the bearer interface (and intervening multiplexers, etc), to the remote processor card and remote monitor.

6.2.4.9 Display Terminal Events.

Past and present events can be viewed via the monitor firmware information selections. Each event is labelled and has a time and date stamp.

6.2.4.10 Access for Data Logging Devices.

The monitor module has two communication channels; local area network (LAN) and the RS232 interface.

To allow efficient logging of events, the local network permits the data from all terminals to be funnelled through one RS232 interface. The terminal with the RS232 connected, provides an extra item in the main menu allowing selection of a terminal network ID to enable connection to another terminal on the LAN.

RS232 and terminals engaged by the LAN have the ability to download command and alarm history in textual form. A summary of the current terminal state and the current terminal setup can also be downloaded in textual form.

6.2.4.11 Terminal Testing.

All essential functions within the terminal are automatically tested by the firmware in the monitor module and processor card. A test menu is provided by the monitor firmware to permit a trip command to be initiated by the TEST button on the processor card.

To assist in fault finding, maintenance menus and debug functions are provided that can be used to display data flow between the Monitor module and the Processor card.

***** WARNING *****

Engaging the debug functions may cause undesirable terminal operation. Use only for fault finding. DO NOT leave debug functions running unattended.

6.2.4.12 Dipswitches.

Dip switches are located at the rear of the Monitor front panel PCB which change the operating mode of the Monitor. These switches are used during factory testing and fault finding.

SW-1 off	Allows setup to be changed.
SW-1 on	Run only. Setup and Maintenance are locked out.
SW-2 off	Normal passcode operation.
SW-2 on	No Setup or Operations passcodes required.
SW-3 off	Normal field operation.
SW-3 on	No maintenance passcode required, additional menus for calibration and fault finding.
SW-4	Not connected.

***** WARNING *****

Switches SW-2 and SW-3 should be in the "off" position during normal operation.

6.3 G703 Processor Board.

(refer to schematic diagrams 4-313-222 and 3-313-223 items 1, 2 and 3.)

The prime function of the G703 Processor Board is to interface the Trip I/O boards with the G703 communication bearer. Its secondary function is to communicate with the Monitor Module. This section describes the Processor Board hardware and reference will be made to the schematics.

Schematic 4-313-222 shows the processor sub-board connecting the processor main board to the trip IOs. Schematic 3-313-223 shows the processor main board, item 1 covers the DSP (digital signal processor) section, Item 2 covers the digital communications section, Item 3 covers the voltage reference and the bus interconnection.

The DSP microprocessor chip, IC9 is a TMS320P25. This microprocessor contains internal RAM and PROM for firmware operation.

The I/O address decoding is performed by IC13. Addresses 0 and 1 decodes to OUT1 and OUT2 for write and INP1 and INP2 for read. These signals enable Output and Input ports Bank1 and Bank2. The write at address 3 decode to OUT4 which is used to reset the watchdog IC6.

The watchdog generates a reset on power up and every 1.6s thereafter if the program fails to generate OUT4. MRESET is connected to the test connector PL4 and is used to override the watchdog during testing. The processor can also be reset by TR1 via DSP RESET from the Monitor Module.

The input port tri-state buffers (IC19, IC21, IC23) and output port latches (IC20, IC22, IC24, IC26) handle the I/O to the processor chip. Some of the signals are used off board while others are used on board. The functions of the signals are listed in Table 6.3.
It should be noted that the TRIP and GUARD signals do not share the same device. Further, IC20 and IC22 are initially disabled (OUTEN = high) to prevent the unintended generation of a trip as a result of the random state of these devices at power up.

Resistor networks are used as pull-up or pull-down resistors to ensure a defined state for those signals where the drive is disabled (tri-stated or un-plugged).

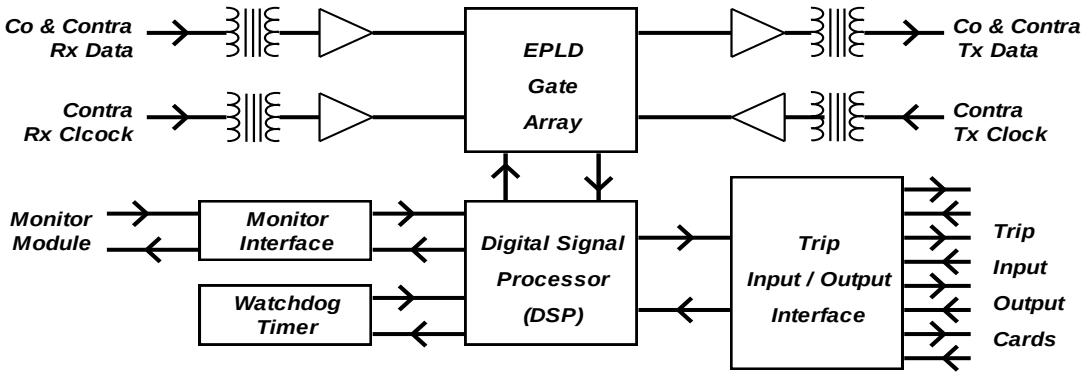

Fig 6.3 G703 Processor Block Diagram.

OUTPUTS

SIGNAL NAME	FUNCTION	LOCATION Bank	Bit
COM ALARM	Drives Common Alarm Relay on PSU	1	0
DSP DOUT	Data from Processor card to Monitor	1	1
DSP DCLK	Clock to Monitor Module for clocking data	1	2
FRAME SYNC	Sync signal to Monitor at start of block	1	3
MON RESET	Provision for reset to the Monitor	1	4
DSP INTER	Provision for handshake with Monitor	1	5
DIG/ANALOG	Configuration signal to IC21 (always 1)	1	6
MAST/SLAVE	Configuration signal to IC21	1	7
O1,O2,O3	Test signals to PL4 pin 7,6,5	1	8,9,10
GUARDOUT 1,2,3,4	Guard drive to Trip I/O cards 1,2,3,4	1	12,13,14,15
CONTRA/CODIR	Configuration signal to IC21	2	0
LOOP/NORMAL	Loop-back control signal to IC20 or IC19	2	1
FO DATA IN	Future option signals to FO. card and Mon	2	2
FO SIG1,3,5,7	Future option signals to FO. card and Mon	2	3,4,5,6
THRESHOLD+	Over threshold input test signal to all T. I/O	2	10
THRESHOLD-	Under threshold input test signal to all T I/O	2	11
TRIPOUT 1,2,3,4	Trip drive to Trip I/O cards 1, 2, 3, 4	2	12,13,14,15

Table 6.3(a) G703 Interface Output Signals

INPUTS

SIGNAL NAME	FUNCTION	LOCATION Bank	Bit
BOOST	From opto-coupler on PSU board	1	0
DSP DIN	Data from Monitor	1	1
I1,I2,I3,I4	Test inputs from PL4 pins 12, 11, 10, 8	1	8,9,2,3
I5,I6	Not used	1	6,7
TEST-SW INV	Test switch, normally high	1	10
GUARD IN 1,2,3,4	Guard inputs from T I/0 cards 1, 2, 3, 4	1	11,12,13,14
FO DATA OUT	Future options signals	2	2
FO SIG 2,4,6	F.O. card and Monitor Module	2	3,4,5
DISCREPANCY 1,2,3	Trip output switch discrepancy signals from all Trip I/O cards.	2	8,9,10
TEST-SW	Test switch, normally low	2	11
TRIPIN 1,2,3,4	Input from Trip I/O cards 1, 2, 3, 4	2	12,13,14,15

Table 6.3(b) G703 Interface Input Signals

6.3.1 Digital Communications Interface.

This section (Schematic Item 2) handles the transfer of data between the processor chip and the digital communications bearer. Four modes of communication are provided:-

Co-directional G703
Contra-directional G703
Master
Loop back

The characteristics of these modes are briefly described.

6.3.1.1 Co-Directional.

In this mode the clock is carried on the same pair as the data as illustrated in Fig 6.1 . Alternate Mark Invert (AMI) coding is used where the signal alternates between positive and negative values with a period of zero value between. A “zero” data bit is represented by two short pulses and a “one” by a long pulse. The start of a block of 8 bits (octet) is indicated by a violation of the alternation rule, ie. two successive data bits of the same polarity.

In this mode the **DEWAR DM1200** extracts the bit clock from the RX Data input and uses it to read the data. In addition the bit clock is used to adjust the frequency of the Phase Locked Loop, IC22, which controls the clock signals used to generate the TX Data. Hence the data into the G703 bearer is frequency locked (but not phase locked) to the data out from the G703 bearer.

6.3.1.2 Contra-Directional.

The contra-directional mode requires that the terminal equipment (DM1200) be supplied with clock signals from the bearer for both receive and transmit functions. The P.L.L. is not used. Although this mode uses less complex signals and decoding hardware, an 8 wire rather than a 4 wire interface is needed.

6.3.1.3 Master.

The previous two modes require that the bearer supply at least one clock signal as a timing reference. The usual application utilises a 64Kb/s port of 2M b/s multiplexer. Where no such equipment exists, eg. where two **DEWAR M1200** terminals are connected by physical pairs, at least one of the terminals must take charge of the timing. In master mode the TX signal conforms to the co-directional standard but the clock is derived from the processor chip clock. The second terminal must operate in co-directional slave mode.

6.3.1.4 Loopback.

Loop back mode represents a single terminal in Master Mode with TX linked to RX to facilitate testing.

6.3.2 Interface Signals.

The two clock signals and the RX Data are all handled in the same way. The line is terminated and coupled to a line receiver, IC17, via a transformer and high frequency noise filter. The detection thresholds are set at +/- 1V. When the input signal (+/- 2.0V peak) crosses the threshold, the line receiver generates a low-going signal.

All the G703 decoding and encoding is performed within the Programmable Logic Device (PLD), IC3. The inputs to this device consist of the mode control signals, the outputs from the 6 line receiver comparators, 10.24MHz processor clock and the PLL output.

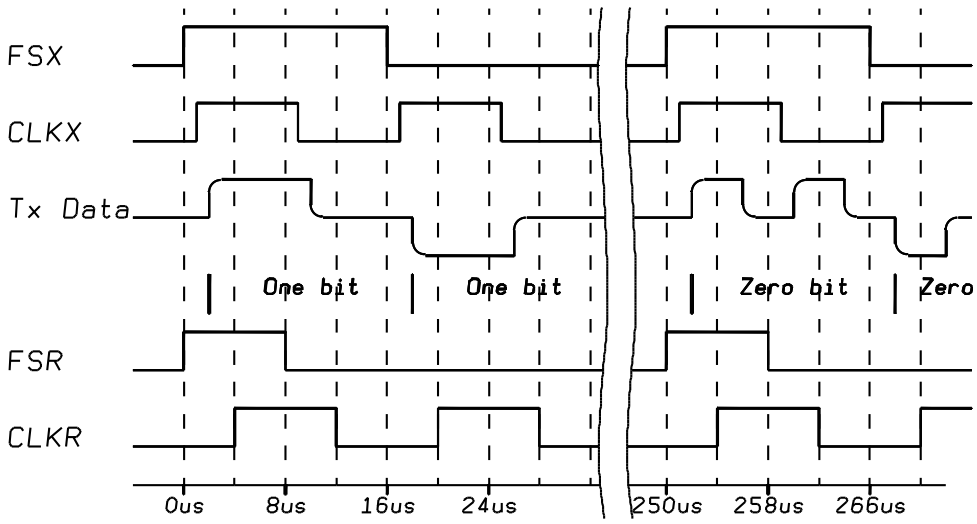

Fig. 6.3.2 Waveforms.

When in co-directional mode the PLD detects the octet framing and generates a 4KHz signal PLLAIN. The PLLOUT signal at 512KHz is divided within the PLD to produce a 4KHz signal, PLLBIN. The PLL causes these two signals to lock in phase. The clock decoding process results in short transients on the PLLAIN signal which are removed by R-C filtering. The DC supply to the PLL is decoupled to isolate it from disturbances on the 5V rail.

Communication between the PLD and the processor chip is via the processor serial ports. The recovered receive clock appears on CLKR which clocks the data, DR, into the serial receive port. Every second octet, the FSR frame sync. pulse is generated to initiate the data transfer.

The transmit operation is similar. The PLD clock, derived from either the processor clock or PLL depending on mode, generates FSX which initiates the output of data, DX, under the control of CLKX. The timing of these signals is indicated in Fig 6.2.

The transmit data is correctly formatted within the PLD as a unipolar signal. The output amplifier, IC28, is switched between inverting and non-inverting by IC20B under the control of POLART to generate the AMI signal.

The line transformer T2 provides some degree of low pass filtering. R29 provides reverse termination for the TX DATA line. The third winding provides the loop-back signal which is selected by IC20A.

Reference was made in the previous section, to the need to disable the Trip and Guard output ports until proper operation of the processor is established. This function can be provided by IC23A, however, the function is duplicated within the PLD. IC23 is fitted only in Models using analogue communications where the PLD is not required. Before power up, C33 is discharged. At power up, the reset generated by the watchdog resets IC23A and OUTEN goes high, disabling the output ports. When the program is running a series of pulses appears at OUT4 and after a time delay, the voltage on C3 is sufficient to cause IC23A to change state, enabling the ports.

6.3.3 Dip-Switches.

There is a four pole switch on the processor board. SW1 determines the location of program memory; “off” for internal DSP memory, “on” if external DSP memory is fitted.

***** WARNING *****

SW1 is factory set during manufacture and is not to be changed

The other switches allow the setting of the communication mode with no Monitor connected to facilitate testing. These switches are read only at power on.

SW2, SW3, SW4 all off: contra-directional .
SW2 on; co-directional slave.
SW3 on; co-directional master.
SW4 on; loop back.

If more than one of the above switches 2, 3. and 4 are on, then the highest number has predence.

6.4 VF Processor Board.

(refer to schematic diagrams 4-313-222 and 3-313-224 items 1, 2, 3 and 4.)

The prime function of the VF Processor Board is to interface the Trip I/O boards with the VF communication bearer. Its secondary function is to communicate with the Monitor Module. This section describes the VF Processor Board hardware and reference will be made to the schematics.

Schematic 4-313-222 shows the processor sub-board connecting the processor main board to the trip IOs. Schematic 3-313-224 shows the processor main board, item 1 covers the microprocessor section, Item 2 covers the pilot line interface and the bus interconnection section, Item 3 covers channel 1 transmitter and receiver, item 4 covers channel 2 transmitter and receiver.

The VF processor is constructed on a 4 layer PCB. The middle two layers are the +5 volts power plane and the ground plane. The internal planes reduce crosstalk, RFI and stray signal pickup in the processor.

The VF processor uses many surface mounted integrated circuits. Special care must be taken in replacing these components.

The heart of the VF processor board is a Z182 microprocessor, IC17. The Z182 is clocked by XTAL1, there no internal division of XTAL1 output frequency, the data and address busses operate at the same frequency as XTAL1. This requires high speed EPROM, IC15, and RAM, IC13, to keep pace with IC17.

IC22 buffers the high speed data buss for IC17. RN3 provides buss termination for the high speed input / output ports to the trip IO cards and monitor interface, IC38, IC39, IC40 and IC41, and also to the VF frequency control EPLD's, IC23 and IC25. IC5 and IC7 decode high speed IO port address. Refer table 6.4.

OUTPUTS

SIGNAL NAME	FUNCTION	LOCATION Bank	Bit
COM ALARM	Drives Common Alarm Relay on PSU	1	0
DSP DOUT	Data from Processor card to Monitor	1	1
DSP DCLK	Clock to Monitor Module for clocking data	1	2
FRAME SYNC	Sync signal to Monitor at start of block	1	3
GUARDOUT 1,2,3,4	Guard drive to Trip I/O cards 1,2,3,4	1	4,5,6,7
DSP INTER	Provision for handshake with Monitor	2	0
LOOPBACK	Loop-back control signal to IC20 or IC19	2	1
THRESHOLD+	Over threshold input test signal to all T. I/O	2	2
THRESHOLD-	Under threshold input test signal to all T I/O	2	3
TRIPOUT 1,2,3,4	Trip drive to Trip I/O cards 1, 2, 3, 4	2	4,5,6,7

Table 6.4(a) VF Interface Output Signals

INPUTS

SIGNAL NAME	FUNCTION	LOCATION Bank	Bit
BOOST	From opto-coupler on PSU board	1	0
DSP DIN	Data from Monitor	1	1
TEST-SW INV	Test switch, normally high	1	2
MON-INTER	Monitor Interlock	1	3
GUARD IN 1,2,3,4	Guard inputs from T I/0 cards 1, 2, 3, 4	1	4,5,6,7
DISCREPANCY 1,2,3	Trip output switch discrepancy signals from all Trip I/O cards.	2	0,1,2
TEST-SW	Test switch, normally low	2	3
TRIPIN 1,2,3,4	Input from Trip I/O cards 1, 2, 3, 4	2	4,5,6,7

Table 6.4(b) VF Interface Input Signals

The Z182 microprocessor contains the IO ports to interface the microprocessor to the slow IO devices. The slow IO devices are selected by IC4 and IC6. The slow IO devices are;-

- analogue to digital converter (ADC) IC14,
- digital to analogue converters IC31, IC24, IC34, IC19 and IC38,
- watchdog and calibration EEPROM, IC12.

The power supplies to the analogue sections are separated from the digital sections by VF Supply Filters in IC37, IC36 and associated components, to produce the +5FILT and -5FILT supply rails. The +5FILT rail is the analogue voltage reference.
An RS232 interface is provided for testing and fault finding the VF processor. IC2 and associated components are used for RS232. Appendix D contains details for connecting to VF processor.

A second, low speed, test and fault finding communications channel is also provided through the monitor module.

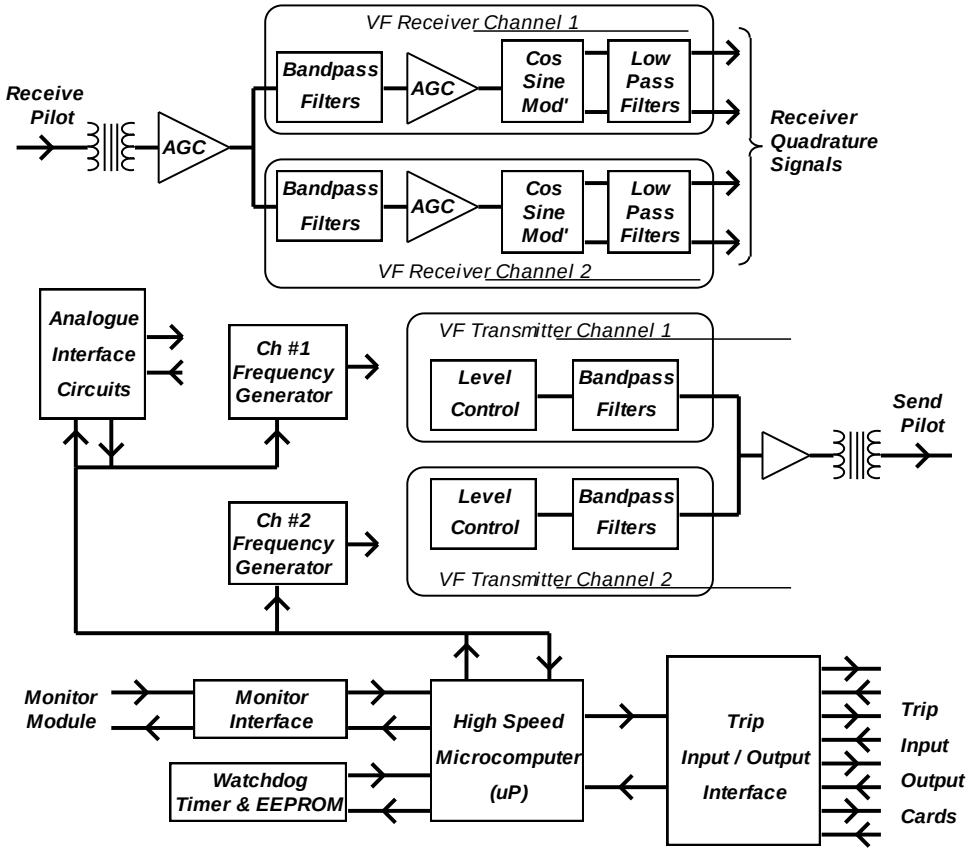

Fig.6.4. VF Processor

NOTE: The VF processor contains two FSK channels. To simplify the operational description of elements on each channel, references to channel 2 components are shown in brackets, eg. (IC23) is part of channel 2.

6.4.1 Send Pilot Interface.

The two transmitter TX Bandpass Filter outputs are combined by the TX Line Driver, IC35: A. The driver operates in current mode to allow summation with existing line signals.

The transmitter channel level is monitored by TX Level Detector, IC35:D (IC35:C). The send pilot line level is monitored by TX Line Detector IC35:B.

The send pilot is isolated from internal terminal levels by T1. T1 is 150 ohm on the equipment side and 600 ohm line side transformer. C65 provides DC isolation from the TX Line Driver to T1. R67 terminates the send pilot at 600 ohms and provides a DC bias for TX Line Driver output.

Power to the TX Line Driver is filtered by R74, C61 and ZD1 to produce the +12Volt supply rail.

6.4.2 Receive Pilot Interface.

The receive pilot is isolated from the internal terminal signals by T2. The receive pilot is terminated by R76 at 600 ohms. The output of T2 is attenuated by R68 and R78. IC32: A and IC32:C form the analogue loopback switch.

6.4.3 Frequency Control.

Transmit and receive frequencies are derived from XTAL1, 24.576 MHz. An EPLD, IC23 (IC25), generates all VF frequencies. The software controls the frequencies generated by EPLD by sending selection data to ports on the EPLD.

The EPLDs are programmed in circuit during calibration. The EPLD's use EEPROM technology and are non-volatile.

6.4.4 Transmitters.

Each transmitter produces sinusoidal waveforms of the required frequency and level. The transmitter outputs is passed to the TX Line Driver for transmission on the send pilot.

6.4.4.1 Level Control.

The transmitter level is controlled by TX Send Level DAC, IC38 (IC34). The microprocessor software sets the DAC value according to calibration data, to the required user level.

The transmitter fundamental frequency is supplied from the EPLD IC23 (IC25), in square wave form, to the reference pin of the TX Send Level DAC.

The output from the TX Send Level DAC is filtered by R41 (R58) and C45 (C59) to reduce high frequency harmonics before being output to the transmitter bandpass filters.

6.4.4.2 Bandpass Filtering.

The output from the TX Send Level DAC filtering is processed by the TX Bandpass Filter, IC29 (IC28).

The TX Bandpass Filter reduces harmonics, leaving a sinusoidal waveform at the fundamental frequency and proportional to the required output level.

6.4.5 Receivers.

The received signal from the loopback selector, IC32:C and IC32:A.

6.4.5.1 Line AGC.

The received signal level to the RX Bandpass Filters is controlled by the RX Level Control DAC, IC31 and its associated op-amp circuitry on IC33:D. The level of the output of IC33:D is monitored by the RX Line Detector, IC33:C. The output of RX Line Detector is converted to digital form by the ADC and passed to the microprocessor firmware for analysis. The microprocessor firmware then sets the RX Level Control DAC, to present the RX Bandpass Filters with a gain adjusted receive signal.

6.4.5.2 Bandpass Filtering.

The RX Bandpass Filters, IC21 (IC26) and IC20 (IC27), provides basic filtering to reduce adjacent channel levels.

The bandwidth of the filters can be set up by the user or left at the default setting.

If a bandwidth is setup, the filter sections are used to control the channel automatic gain control, AGC. This allows the filters to follow signals down to 20 dB below adjacent channels and stopping the RX product detectors being saturated with unwanted signals. The filter group delay will extend as the filters pass band tightens, causing the trip response time to increase. The accuracy of receiver level calculated from the RX Low pass filter outputs will be +/-5 dB, as the gain of the RX Bandpass Filters increases. This is due to the effect of compounded tolerance variation in bandpass filter chips.

The frequency of operation of the RX Bandpass Filters is controlled clocks at 64 times or 128 times the received signal. The clock is generated by the EPLD.

6.4.5.3 Channel AGC.

The receiver channel automatic gain control (AGC) is implemented in two ways;-

- by the RX Gain Control DAC, IC19 (IC24), only when the RX Bandpass Filter use the default bandwidth setting,
- by the RX Bandpass filters when the user sets up a bandwidth the bandpass filters. The setup response time of the bandpass filters is slow. To keep the signal in dynamic range, the RX Gain Control DAC is also used to trim the signal level during signal level variations.

The channel AGC provides the RX Product Detector input.

6.4.5.4 Channel Mixers.

Each channel has two mixers, one sine IC11 (IC18) and one cosine IC3 (IC16), used as product detectors. The RX Product Detectors use balanced demodulation integrated circuits.

The local oscillator (LO) references for sine and cosine demodulators are generated by the EPLD at the channel centre frequency. The two references are in quadrature, to provide the sine and cosine outputs.

The demodulator output contains the LO plus received frequency and LO minus received frequency, the received frequency and LO components being removed by the balanced operation of the demodulator. The demodulator output is filtered by C7 (C26) and C20 (C17) to reduce high frequency LO harmonics. C21 (C27) and C19 (C18) removes DC components from the demodulator output.

6.4.5.5 Channel Low Pass Filters.

Each channel has two, one sine IC1 (IC8) and one cosine IC3 (IC9), low pass filters. The outputs from the channel mixers are filtered to produce two sinusoidal outputs in quadrature. The frequency output is the difference between the LO and the received signal.

The cut-off frequency of the RX Lowpass Filters is controlled by a clock produced by the EPLD. The clock frequency is 100 times the required cut off frequency. The cut off frequency used is 0.5 or 0.6 times the expected shift frequency. The selection of which cut off frequency is controlled by calibration settings.

The RX Lowpass Filters provide the receiver with the required selectivity to reject adjacent channels.

6.4.6 Analogue to Digital Converter (ADC).

All voltage inputs to the VF processor software are converted to digital form by the ADC IC14. The reference to the ADC is the +5FILT supply rail. The ADC has unipolar / bipolar operation and has 12 bits of resolution.

6.4.7 Calibration.

The VF processor calibration process is software controlled. The software requires a terminal be connected to the processor RS232 port or View Processor is selected on the monitor module.

The calibration process tests and sets the following;-

- test the EEPROM and watchdog timer, IC12.
- inputs module setup variables including filter chip type, AGC response time, low pass filter cut off, number of FFT points, EPROM speed, RAM speed, etc.
- verifies the programming of the EPLD's. It not correct, the EPLD’s are erased and programmed.
- calibrates the TX Line Detector and RX Line Detector.
- calibrates TX1 Level Detector, TX2 Level Detector and transmitter level setting functions.
- calibrates each channel's receiver levels.
- save the calibration settings in EEPROM.
- test the trip IO card interface.
- check self test operation.

The calibration process requires inputs from the operator of true RMS millivolts. Each calibrated item has four measured points. These points are used as a reference by interpolation, during VF processor operation, to convert raw digital information to voltages and vice-versa.

The internal code for the EPLD' s is stored in the microprocessor firmware EPROM, IC15. It is not necessary to remove the EPLD's for erasure or programming. The devices are in-circuit programmable.

After any component replacement on the VF processor card should be re-calibrated. This is the suggested method for determining the status of the processor after repair.

6.5 Trip I/O Board.

The Trip I/O board interfaces one trip input circuit and three trip output circuit "contacts".

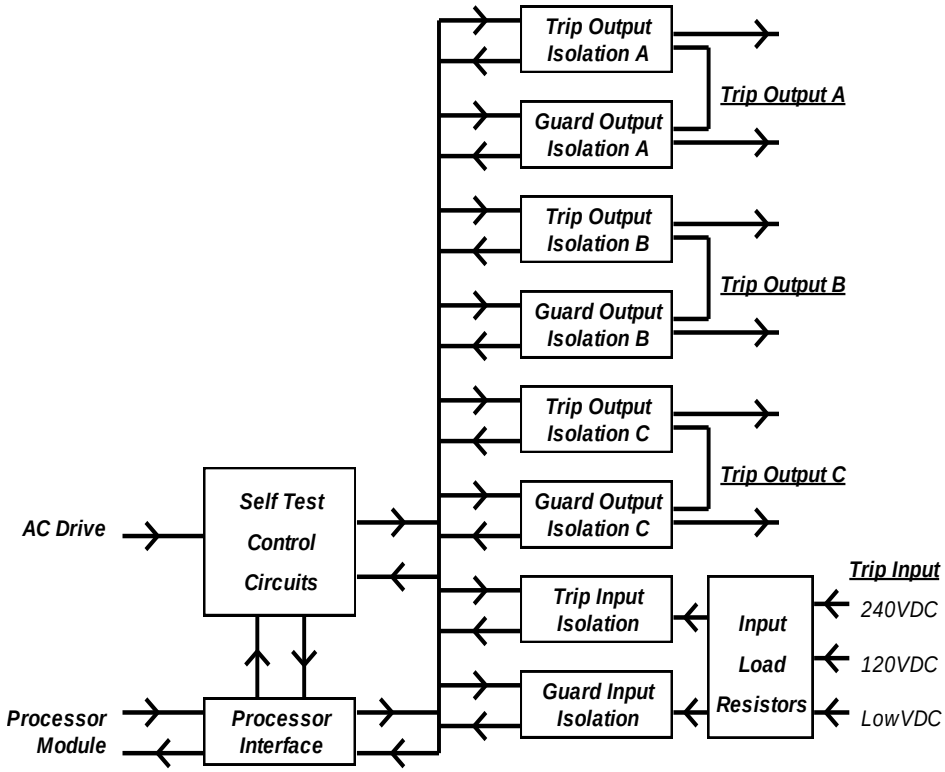

Fig 6.5 Trip IO Card Block Diagram.

6.5.1 Trip Input.

(refer DWG. 3-313-321, Item 1.)

The trip inputs are protected from voltage transients by MOV's, alternatively transorbs. The resistor network connected to each of the three input terminals provides the appropriate load current. LK1 and LK2 allow programming of the lower voltage terminal. When the input current approaches the nominal value, the voltage at the cathode of ZD7 is sufficient to cause a portion of this current to be shunted through the opto-isolators IC13, IC14. The opto outputs are ported to the Processor board. Current can be injected via D12 into the network for self test (see 6.4.3). D10 prevents this test current from being fed into the lower voltage input circuits. The resistance in the 240 V circuit is sufficiently high to make isolation unnecessary.

6.5.2 Trip Output.

(refer DWG. 3-313-321, Item 2.)

Three identical solid state **contacts** are provided. Output 1 will be described. An active trip signal switches on TR5 (refer item 1.) which drives opto-couplers IC4, IC6, IC9. Similarly, a non-active guard drives IC3, IC7, IC11. The AC Drive from the Power Supply excites the primary winding of T1. The six isolated secondary windings (refer item 2.) provide power to energise the three SSR circuits.

The SSR consists of two series connected transistors TR1, TR2. These may be FET's or IGBT's, depending on the current rating. Each transistor is protected by a MOV or transorb. The opto-coupler switches the gate of the transistor.

The remainder of the circuit is associated with self testing.

6.5.3 Self Test.

The input and output sections of the card each have an associated self test circuit. The function of the input self test is to inject two levels of current into the trip input. The levels represent values below and above input threshold.

If these currents were to be supplied at normal trip input voltage, a high power level would be involved. Additionally there is the complication of the differing trip input voltages. Consequently, the current is injected after the dropping resistors, where the voltage is 8V. The reason for leaving the dropping resistors out of the testing loop, is that should a resistor fail, it will invariably do so to an open circuit condition (which will not result in a false trip) rather than to a short circuit condition.

The current is supplied through transformer T2 and rectified by the doubler C22, D11, D12.(item 1). The current is regulated by controlling the primary current. The AC primary current is rectified in a similar doubler circuit to provide a floating DC output. The current is switched on and off by TR10 connected to the +ve. output while the current is regulated by TR11 (grounded base connected) to a value approaching that of the current injected into its emitter. With TR9 off, this current corresponds to the under threshold value while with TR9 on, an over threshold value is established.

The function of the output self test is to determine whether the two transistors comprising the SSR (item 2) are in the same state. The resistors in networks RN1, RN2 and TR1, TR2 form a bridge. Provided there is a voltage applied to the trip output terminals and the transistors are off, the voltage at the inputs to the comparators will keep their outputs high. In the absence of voltage across the output terminals, the small bias derived form R2, R3 keeps the comparator outputs high. If however there is a substantial difference in the transistor voltages, one of the comparators will go low turning on opto-coupler IC2. This results in a low active signal being applied to the DISCREPANCY1 output pin of the card. This signal is interpreted by the Processor card.

6.6 Power Supply.

(refer diagrams 3-313-424 and 3-313-425).

The functions of the power supply is to provide:-

1. An isolation barrier between the user's battery and the terminal,
2. Supply regulated DC voltages and a high frequency AC voltage to power the system,
3. ‘Boost Input’ interface (for analogue systems),
4. Common Alarm’ relay interface.

The power supply consists of a flyback DC to DC converter using a UC3645 SMPS controller device.

Over current and transient voltage protection and inrush current limitation are provided by FS1, ZV1 and TH1. RFI filtering is provided by C10, C13, L3 and L4. D4 (1200-42) or BR1 (1200-43) provides reverse polarity protection.

At power up, the supply for IC1 is provided via R2 or R3. Once the converter is running, supply is obtained from T1 via D6. If the supply voltage drops below 7 volts, IC1 will go into stand by mode until the voltage on C9 returns to a value above 9 volts, and then will start up.

The maximum duty cycle is limited in IC1 internally to 50 percent. Maximum current through TR1 is controlled by the current feed back provided from R13 to pin 3 of IC1.

Under normal operation, the duty cycle will increase until the output reaches the required voltage, further increase being controlled by the feedback signal on IC1 pin 2.

The frequency of operation of IC1 is controlled by R7 and C7. This is typically 50 kilohertz.

The feedback applied to IC1 pin2 is gain compensated. IC1 pin 1 has AC feedback and DC clamping applied by C6, D1, D2, R8 and R4. This allows stable PSU feedback under normal load levels.

The forward voltage, rectified by D10 and scaled by R17, R18 is used by the Monitor module to monitor the battery voltage. The flyback voltage is rectified to provide three output voltages. The duty cycle of the converter is controlled to provide regulation of the 5V rail, the other outputs being only partly regulated.

Differential amplifier, TR2 and TR3, compares the voltage of the 2.5 volt reference, IC3, with the voltage at the junction of R23 and R28 to control the current through the feedback opto-coupler, IC2. When the voltage at pin 4 of IC2 exceeds 2.5V, the duty cycle is reduced.

The +5 volt output current is sensed across R31 and when this voltage exceeds approximately 0.7 volts, TR4 turns on, increasing the current flowing through IC2.

The -8 volts is regulated by a standard 3 terminal regulator IC7.

The +12 volt is regulated by a standard 3 terminal regulator IC4. To reduce heat on the heatsink of IC4, R29A and

R29B reduce the input voltage to IC4, thus reducing the heat generated by IC4.

Output over voltage protection crowbars are provided by SCR1, SCR2, SCR3 and their associated components.

To provide AC power for the trip IO cards, IC4 produces a 125KHz square wave. The output of IC5 pin 6 is boosted by the complimentary switch mode amplifier to provide 18V p-p.

The Boost input is protected from transient voltage spikes by ZV2. R44 limits the current into IC6:B. D12 protects IC6:B from reverse polarity connected signals.

The Common alarm output from the terminal is provided by RL1. TR9 amplifies the logic signal from the internal terminal circuits. ZV3 through ZV6 provide protection for relay contacts.

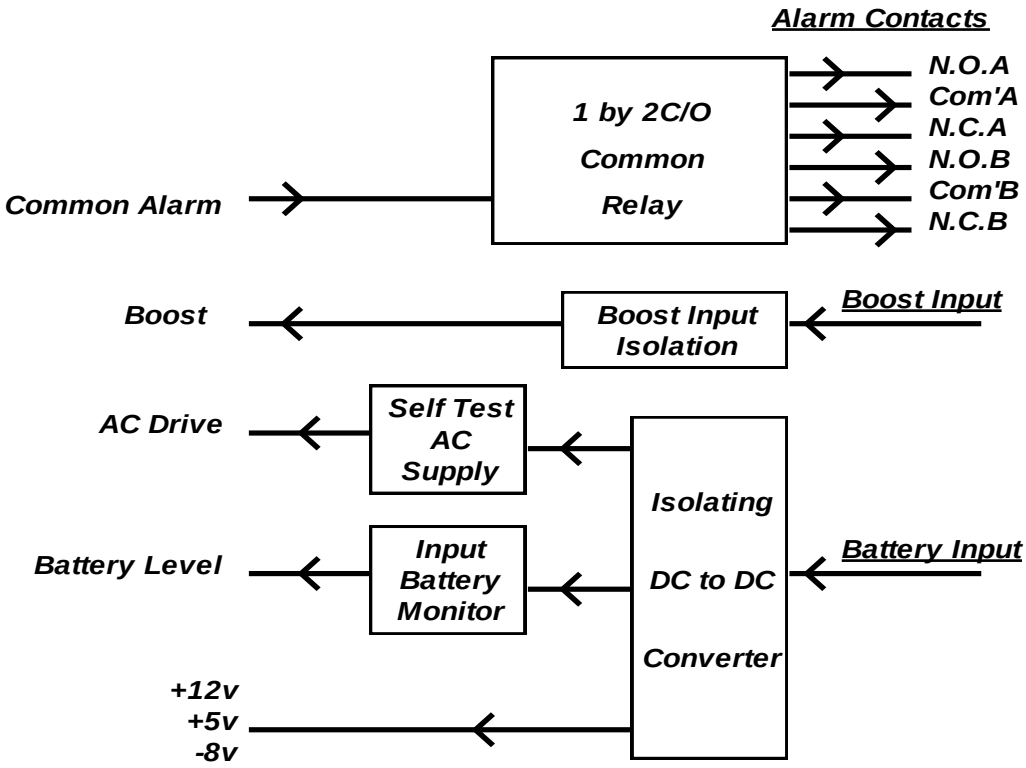

Fig 6.6 Power Supply Block Diagram.

6.7 Firmware.

Explanation. The term “firmware” is used where software is fitted to hardware. This implies that software cannot be altered by the terminal hardware alone. To alter firmware, the IC has to be physically removed from the terminal, erased and reprogrammed. Flash upgrades are possible where on some modules via DM1200TALK.

An overview of the firmware is provided. Firmware listings are proprietary information and are not included.

Modular programming has been employed in all firmware used on the DM1200. These modules allow a hierarchy of firmware execution, from physical interface to hardware at the lowest level up to the application program at the top level.

6.7.1 G703 Processor Firmware.

On reset, the G703 processor tests for the presence of the Monitor module. If absent, default system operating parameters are loaded and the communication mode read from DIP switches. The program then loops awaiting interrupts from the G703 serial ports. The loop maintains the clocks that control the system timing.

The monitor module must send a G703 ready signal before the G703 processor can process command information. This stops incorrect setup (eg. setup is for a VF processor) being interpreted by the G703 Processor.

During execution the G703 processor carries out continuous self tests on the trip IO cards.

6.7.2 VF Processor Firmware.

On reset, the VF processor checks the validity of the calibration tables, and EPROM checksum, the processor then waits for the Monitor module to transfer a valid setup. If valid, the processor calculates the filter and DAC settings and sets these values into the hardware registers. When all setup to the hardware is complete the monitor module allows processor operation, the VF processor then starts the VF transmitters.

The monitor module must send a VF ‘ready’ signal before the VF processor can process command information. This stops incorrect setup (eg. setup is for a G703 processor) being interpreted by the VF processor. The VF processor returns the VF ready signal if no errors are found in the VF processor EPROM or calibration.

During execution of the VF processor, the hardware registers in the filters and DAC’s are reloaded periodically to maintain correct operation.

During execution the VF processor carries out self tests on the trip IO cards.

6.7.3 Monitor Module Firmware.

On reset, the monitor module checks the validity of the real time clock, setup values and EPROM check sum. If valid, the monitor module transfers the setup data to processor.

The monitor module continuously checks the terminal parameters. If terminal conditions are correct (eg. no monitor fault alarm), the monitor send a VF or G703 ready signal to the processor, according to the type of setup stored.

During execution, the monitor continuously self checks and resends the setup data to the processor.

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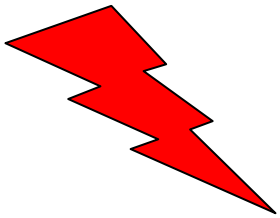
SECTION 7

Maintenance.



DANGER

Dangerous voltage levels are present within the DM1200 Teleprotection Terminal. Trained and competent technicians should undertake maintenance. All work should be conducted with extreme care and due diligence

Refer to Principles of Operation. Section 6

Power should be disconnected prior to removal of any module.

There is no requirement for routine maintenance. Failure of the Processor or Trip I/O cards or deterioration of the Power supply is reported to the LCD. A catastrophic failure of the Monitor or Power Supply modules cannot be reported to the LCD, however all alarm relays will release. First level corrective maintenance should be performed by card replacement.

The Maintenance menu can be of assistance in fault finding (refer Appendix A) unless a catastrophic failure occurs.

The VF processor has a range of diagnostic displays available via a RS232 connection the VF processors RS232 port or via the "MAINTENANCE MENU" "VIEW PROCESSOR". Type [H] on the keyboard brings up the help screen.

When components are replaced on the VF processor, it is essential that the VF processor calibration process be carried out. The calibration process is an automated test procedure.

7.1 EXTENDERS

Two types of extender are available to assist in repair. Type **X2** (1200-70) consists of a card that fits into the terminal with sockets to hold the card under test clear of the terminal. Type **X1** (1200-71) consists of the same card cut in two with the sections joined by ribbon cable. This type is preferred for bench use.

All the tracks on the extenders are fitted with test pins that are identified by the corresponding connector designation. In addition, the signal names for the Processor slot are identified. Not all the signal names will be correct in other slots.

Caution

The X1 bench extender may cause interference from the AC drive to 5 volt signals.

It is recommended that the clock battery in the Monitor module be replaced every 10 years while a unit is in service. Since the clock battery supplies power only while the unit is out of service, units in long term storage (ie. greater than 6 months) should have the battery removed or a new battery fitted when returned to service.

7.2 SCHEMATICS.

3-313-126 Item 1.	Model 1200-10B, Monitor Module, CPU section.
3-313-126 Item 2.	Model 1200-10B, Monitor Module, Discrete I/O.
3-313-122	Model 1200-10, Monitor Module Front Panel Interface.
3-313-123	Model 1200-12, Alarm Relay Card Schematic.
4-313-222	Model 1200-21, G703 and VF Processor Sub-board
3-313-223 Item 1.	Model 1200-21, G703 Processor D.S.P.
3-313-223 Item 2.	Model 1200-21, G703 Processor Schematic, G703 Data Section.
3-313-223 Item 3.	Model 1200-21, G703 Processor Schematic, Miscellaneous Section.
3-313-224 Item 1	Model 1200-22, VF & CPU Processor
3-313-224 Item 2	Model 1200-22, VF Processor, and Pilot Line
3-313-224 Item 3	Model 1200-22, VF Processor Channel #1 TX and RX
3-313-224 Item 4	Model 1200-22, VF Processor Channel #2 TX and RX
3-313-323 Item 1.	Model 1200-32, Trip I/O Card Trip Input and Interface.
3-313-323 Item 2.	Model 1200-32, Trip I/O Card Trip Output
3-313-424	Model 1200-42, 20 to 60 VDC Power Supply
3-313-425	Model 1200-43, 90 to 320 Volts Power Supply
4-313-423	Model 1200 PSU Test Rig.
3-313-521	Model 1200, Terminal Board
3-313-522	Model 1200, Buss Board

7.3 DIAGRAMS

3-313-548	Model 1200 Terminal and Wiring Layout Diagram.
4-313-82	Model 1200 Terminal Dimensions Diagram.

7.4 MATERIAL LISTS.

P-0313-0106	1200-10B Module, Monitor.
P-0313-0116	1200-10B PCB Assembly, Monitor.
P-0313-0112	1200-10 PCB Assembly, Monitor Front Panel.
P-0313-0114	1200-12 PCB Assembly, Alarm Relays 8 by Single Changeover.
P-0313-0202	1200-21 Final Assembly, G703 Communications.
P-0313-0203	1200-22 Final Assembly, VF Communications.
P-0313-0212	1200-20 PCB Assembly, Processor Sub-Board.
P-0313-0213	1200-21 PCB Assembly, G703 Communications.
P-0313-0214	1200-22 PCB Assembly, VF Communications.
P-0313-0313	1200-33 PCB Assembly, Trip I/O, 340V/2.0A Output.
P-0313-0414	1200-42 PCB Assembly, Power Supply, 20 to 60VDC.
P-0313-0415	1200-43 PCB Assembly, Power Supply, 90 to 320Volts.
P-0313-0501	1200-50 Terminal Assembly, with Motherboards.
P-0313-0511	1200-50 Terminal Metalwork Assembly
P-0313-0512	1200-50 PCB Assembly, Outer Motherboard for User Termination.
P-0313-0513	1200-50 PCB Assembly, Inner Motherboard for Internal Signals.
P-0313-0701	1200-70 One Piece Extender Card Assembly
P-0313-0702	1200-71 Cabled Extender Card Assembly
P-0313-0711	1200-70 One Piece Extender Main PCB Assembly
P-0313-0712	1200-71 Cabled Extender Outer Main PCB Assembly
P-0313-0713	1200-71 Cabled Extender Inner Main PCB Assembly
P-0313-0714	1200-70 & -71 Extender Inner Sub-board PCB Assembly
P-0313-0715	1200-70 & -71 Extender Outer Sub-board PCB Assembly

APPENDIX A

Menu structure.

All menus are hierarchical. The root menu in the hierarchy in the "MAIN MENU". From the "MAIN MENU" all other menus are accessible. The menus and selections are self explanatory, as far as possible within the scope of the display in use.

Menus displayed on the front panel LCD are displayed in a reduced form. Menus displayed on PC screen via RS232, LAN or modem connections, show more information.

Menu Level Conventions.

Each menu and selection in the menu hierarchy has a unique menu level. The level is indicated on the top line of the display. On the LCD the level displayed may be limited by the available display width. For example;-

Level 3.4 **4 Date & Time**

Level 3 **3 Information** menu, level 3.4 is the **Date & Time** selection in the information menu.

The "MAIN MENU" is level '0'.

The contents of menus will change depending upon the options fitted and the current setup. However the index on the left of the menu selection remains constant.

Navigating Menus.

Wherever possible, the information displayed is self explanatory. The number of menus, type of selections and number of variables available for display is very large and is not reproduced in this manual. More information can be obtained by pressing [F1] when on the PC running 1200TALK is connected to a DM1200 terminal.

Using Front Panel Keypads and Liquid Crystal Display (LCD).

The user moves from selection to selection on the LCD by pressing the [↑], [↓], [←] and [→] keypads. The selection is made by pressing [↵]. The menu can be exited by pressing the [ESC]. The keypad has an automatic repeat function. Pressing the keypad for more than 0.75 seconds initiates the auto repeat feature, repeating the same key five times a second.

LCD Menu.

`-- TITLE -- 3`	Title line	also shows menu level (eg 3) if room on LCD.
`4 Fourth Selection`	Next item up	the last item in menu wrapped around.
`5 Fifth Selection`	Present selection	indicated by cursor.
`6 Sixth Selection`	Next item down.	NOTE: No help is available on the LCD.

LCD Numerical Input Display.

`-- HOLD-OFF TIME --`	first line is heading or title line.
`Set time (seconds)`	second line is the unit description (eg. seconds).
`0.02 (step 0.01)`	third line has the value being entered and key step size..
`Change- cursor keys`	fourth line has a short message.

This example shows a typical numerical input display.
The [↑] and [↓] are used to add and subtract the step size from the value.
The [→] and [←] increase and decrease the step size by a factor of ten.
Pressing [**ESC**] aborts the input display and leaves the value unchanged.

Pressing [↵] saves the changes.
The value is limited to between the minimum and maximum

LCD Time and Text Input Display.

- SET DATE/TIME -	first line is heading or title line.
DD/MM/YYYY	second line is a short help message (eg. The date format).
Set Date 14/12/2001	third line has the digits or text being entered.
Change- cursor keys	fourth line has a short message.

This example shows a typical text input display.
The [→] and [←] are used to position the cursor over the digit or letter to change.
The [↑] and [↓] are used to rotate the digit or letter up and down through a sequence of digits or letters.
Pressing [**ESC**] aborts the input display and leaves the value unchanged.
Pressing [↵] saves the changes.

Using a PC Keyboard and Screen.

To use a PC (or Laptop) keyboard and screen the DM1200 terminal needs to be connected to the PC's COM port and 1200TALK is running on the PC. See appendix C.

The operation of the menus and input displays on a PC of the front panel keypad and LCD operations, but in a more decorated forms. The advantages of using a PC are;-
Full screen display available.
Full keyboard available.
Direct entry values and text.
Spreadsheet style setup displays.
Help linked to the displayed information.
On screen setup warnings.
Downloading and uploading of setup files, status files and event logs.

PC Menu.

-- TITLE -- (IDnn Level 3) ALARM(s) TRIP(s)	Title line on PC display.
	This example shows LAN ID number 'nn', menu level 3, and that alarm and trip events are present.
0 Exit	This selection is used return 1 level back through the menu hierarchy (same as pressing [ESC]).
1 First Selection	menu item 1, use the cursor keys to select required item
2 Second Selection	menu item 2, or type the last digit of the required selection
4 Fourth Selection	Note that 3 has been skipped, see above.
**** 5 Fifth Selection ****	** marks the current selection that will entered when [enter] is pressed.
6 Sixth Selection	Pressing [F1] will bring up a help message for the current selection.

PC Numeric Input Display.

-- HOLD-OFF TIME -- (IDnn Level 2.6)	first line is heading or title line.
Set time (seconds)	second line is the unit description (eg. seconds).
0.02 (step 0.01)	third line has the value being entered.
0.01min 200.00max	four line to show the minimum and maximum values.

PC Time and Text Input Display.

- SET DATE/TIME - (IDnn Level 2.11.2.1)	first line is heading or title line.
DD/MM/YYYY	second line is a short help message (eg. The date format).
Set Date 14/12/2001	third line has the digits or text being entered.
Change- cursor keys	fourth line has a short message.

PC Spreadsheet Style.

The spreadsheet style displays are enabled by default. The spreadsheet style displays can be enabled and disabled from the ”Set Local Options” menu in the “Information” menu.

```
-- TRIP INPUT CONTROLS -- (ID03  Level 2F.1)
```

first line is heading or title line.

Input 1	Debounce 1	Input 1 Ext'	Guard to Trip	Trip to Guard
ON	1.00 mS	100 mS	1.5 mS	100.5 mS
Input 2	**Debounce 2**	**Input 2 Ext'**	**Guard to Trip**	**Trip to Guard**
OFF	1.00 mS	100 mS	NotUsed	NotUsed
Input 3	**Debounce 3**	**Input 3 Ext'**	**Guard to Trip**	**Trip to Guard**
OFF	1.00 mS	100 mS	NotUsed	NotUsed
Input 4	**Debounce 4**	**Input 4 Ext'**	**Guard to Trip**	**Trip to Guard**
ON	1.00 mS	100 mS	1.5 mS	100.5 mS

```
Input CCTs
Auto Set


Cursor keys to move, [T] toggle ON <-> OFF,
[ENTER] to change, [R] redraw, [ESC] to leave.
```

In this example, the current selection is highlighted (eg ON). At the bottom of the screen are short messages to help the operator navigate and change settings. Where a displayed item is read only, the operator cannot change the value (eg response times calculated from the settings). Each item has help message relating to the selected item. Pressing [F1] displays the help message.

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APPENDIX B

Factory Defaults.

The 'SET DEFAULTS' menu selection senses the type of processor fitted in the terminal or follows the G703, RS422 or VF mode settings depending upon the previous menu selections. An “AUTODETECT” selection provides an easy means of setting hardware dependant settings.

All of the default settings have three performance levels, “HIGH SECURITY”, “OPTIMUM” and “HIGH SPEED”. The “HIGH SECURITY” is intended for direct tripping schemes. The “OPTIMUM” is intended for permissive intertripping schemes. The “HIGH SPEED” is intended for blocking schemes.

After setting up a default, the operator may adjust settings as required. But after setting a default for a particular performance level, the firmware will not let the operator set new values which are outside the performance level requirements. If the operator needs to have a setting that is outside the performance level requirements, the performance level can be manually changed to accommodate the requirements.

Default Settings for G703 Communications

Table A1 G702 Default Settings

G703 IO Timing:-	**High Security**	**Optimum**	**High Speed**
Debounce time #1, #2, #3, #4	1 ms.	1 ms.	1 ms.
Input extend time #1, #2, #3, #4	100 ms.	100 ms.	0
Output extend time #1, #2, #3, #4	100 ms.	100 ms.	0
Hold Off time	10 ms	10 ms	0
Cut Off time	0	0	0

G703 Communications :-	**High Security**	**Optimum**	**High Speed**
Mode (if not auto detected)	CO-DIR, SLAVE Octet Framing	CO-DIR, SLAVE Octet Framing	CO-DIR, SLAVE Octet Framing
Security / dependability	N = 6, M = 8	N = 4, M = 8	N = 1, M = 2
Identity Checking	Disabled	Disabled	Disabled
BER Threshold	100	100	100

G703 Trip I/O Usage:- Common to all default G703 performance settings	.
TRIP #1 (if not auto detected)	circuits ‘ABC’ on trip I/O module 1, no SIT
TRIP #2, #3, #4 (if not auto detected)	‘Nil’ circuits on trip I/O modules 2, 3 and 4

G703 Alarm relay allocation:- Common to all default G703 performance settings.

Alarm Source	Relay	Onset	Com’n Alarm	Latching	Relay State
LOSS OF RECD SIGNAL	Relay # 1,	1 second	Include	Disabled	OFF
AIS CONDITION	Relay # 1,	1 second	Include	Disabled	OFF
HIGH BIT ERROR RATE	Relay # 1,	1 second	Include	Disabled	OFF
IDENT FAIL	Relay # 1,	1 second	Include	Disabled	OFF
TRIP 1,2,3,4 INPUT FAULT	Relay # 2,	1 second	Include	Disabled	OFF
TRIP 1,2,3,4 OUT FAULT	Relay # 2,	1 second	Include	Disabled	OFF
TRIP#1 REC'D Copy	Relay # 3,	0	Exclude	Disabled	ON
TRIP#2 REC'D Copy	Relay # 3,	0	Exclude	Disabled	ON
TRIP#3 REC'D Copy	Relay # 3,	0	Exclude	Disabled	ON
TRIP#4 REC'D Copy	Relay # 3,	0	Exclude	Disabled	ON
POWER SUPPLY WARNING	Relay # 4,	1 second	Include	Disabled	OFF
REMOTE TERM' FAIL	Relay # 5,	1 second	Include	Disabled	OFF
MONITOR FAULT	Relay # 6,	1 second	Include	Disabled	OFF

PROCESSOR FAULT	Relay # 6,	1 second	Include	Disabled	OFF
OFF NORMAL	Relay # 7,	1 second	Include	Disabled	OFF
TRIP#1 SENT Copy	Relay # 8,	0	Exclude	Disabled	ON
TRIP#2 SENT Copy	Relay # 8,	0	Exclude	Disabled	ON
TRIP#3 SENT Copy	Relay # 8,	0	Exclude	Disabled	ON
TRIP#4 SENT Copy	Relay # 8,	0	Exclude	Disabled	ON
TRIP 1,2,3,4 CUT-OFF	Relay # 10,	1 second	Include	Disabled	OFF
TRIP 1,2,3,4 HOLD-OFF	Relay # 10,	1 second	Include	Disabled	OFF
POWER FAIL	Not allocated,	0	Exclude	Disabled	NA
ACCESS	Not allocated,	1 second	Exclude	Disabled	NA
COMMON ALARM Copy	Not allocated,	1 second	Exclude	Disabled	NA

NOTE 1: Alarms with the 'Copy' suffix indicates alarms that are repeated from another event source (i.e. trip commands or the common alarm relay).
NOTE 2: Where the relay is not fitted, the relay allocation is changed to 'Not allocated'.

Default Settings for VF Communications

Table A3 VF Default Settings

VF IO Timing:-	High Security	Optimum	High Speed
Debounce time #1, #2	0.25 ms.	0.25 ms.	0.25 ms.
Input extend time #1, #2	100 ms.	100 ms.	0
Output extend time #1, #2	100 ms.	100 ms.	0
Hold Off time	10 ms	10 ms	0
Cut Off time	0	0	0

Common VF Communications Setiings:-	**High Security**	**Optimum**	**High Speed**
Supervisory link	Enabled	Enabled	Enabled
TX Boost Option	No boost	No boost	No boost
TX channel #1, #2 nominal level	-5.0 dBm	-5.0 dBm	-5.0 dBm
TX channel #1, #2 boost level	0 dBm	0 dBm	0 dBm
TX channel #1, #2 Bandpass	0 (use default)	0 (use default)	0 (use default)
RX channel #1, #2 Bandpass	0 (use default)	0 (use default)	0 (use default)
RX channel #1, #2 high alarm	+4.0 dBm	+4.0 dBm	+4.0 dBm
RX channel #1, #2 low alarm	-15.0 dBm	-15.0 dBm	-15.0 dBm
RX channel #1, #2 correl' time	10 mS	10 mS	10 mS
RX channel #1, #2 hysteresis bias	OFF	OFF	OFF
RX channel #1, #2 wide inhibit	ON	ON	ON
RX channel #1, #2 inhibit trig'	Anded	Anded	Anded
RX channel #1, #2 inhibit to guard	ON	ON	ON
RX channel #1, #2 LoG Output	Nil	Nil	Nil
Identity Checking	Disabled	Disabled	Disabled

NOTE: Setting '0' for the bandpass, causes the VF processor to calculate a default bandpass characteristic that minimises the filter delays and maximumises receiver AGC response. A non zero bandpass value will increase response time and slow down receiver channel AGC response. A non zero bandpass setting allows the user to increase adjacent channel rejection in specialised applications.

VF Dual Channel Communications Settings:-	**High Security 240Hz**	**Optimum 240Hz**	**High Speed 240Hz**	**High Security 480Hz**	**Optimum 480Hz**	**High Speed 480Hz**
TX channel #1 trip input	In #1	In #1	In #1	In #1	In #1	In #1
TX channel #2 trip input	In #1	In #1	In #1	In #1	In #1	In #1
TX channel #1 Guard	1680 Hz	1680 Hz	1680 Hzt	2040 Hz	2040 Hz	2040 Hz
TX channel #1 Trip	1440 Hz	1440 Hz	1440 Hz	1560 Hz	1560 Hz	1560 Hz
TX channel #2 Guard	1920 Hz	1920 Hz	1920 Hz	2520 Hz	2520 Hz	2520 Hz
TX channel #2 Trip	2160 Hz	2160 Hzt	2160 Hz	3000 Hz	3000 Hz	3000 Hz
RX channel #1 Guard	1680 Hz	1680 Hz	1680 Hz	2040 Hz	2040 Hz	2040 Hz
RX channel #1 Trip	1440 Hz	1440 Hz	1440 Hz	1560 Hz	1560 Hz	1560 Hz
RX channel #2 Guard	1920 Hz	1920 Hz	1920 Hz	2520 Hz	2520 Hz	2520 Hz
RX channel #2 Trip	2160 Hz	2160 Hz	2160 Hz	3000 Hz	3000 Hz	3000 Hz
RX thresholds (N / M)	6 / 8	4 / 8	2 / 8	6 / 8	4 / 8	2 / 8
RX channel #1, #2 qualifying time	9 mS	7 mS	4 mS	5 mS	4 mS	2 mS
RX channel #1, #2 inhibit onset	4 mS	3 mS	2 mS	4 mS	3 mS	2 mS
RX channel #1, #2 inhibit extend	50 mS	25 mS	10 mS	50 mS	25 mS	10 mS
RX channel #1, #2 detectors	BOTH	POLY	POLY	BOTH	POLY	POLY
RX channel #1, #2 averaging	ON	ON	OFF	ON	ON	OFF
RX channel #1 trip output	Out #1	Out #1	Out #1	Out #1	Out #1	Out #1
RX channel #2 trip output	Out #1	Out #1	Out #1	Out #1	Out #1	Out #1

NOTE: If two trip IO module are fitted for dual channel operation, the VF defaults will ask if the second trip IO module is required for 'LoG' operation. If one trip IO module is fitted for single channel operation, the second TX/RX chanel is turned off.

VFSingle Channel Communications Settings:-	**High Security 240Hz**	**Optimum 240Hz**	**High Speed 240Hz**	**High Security 480Hz**	**Optimum 480Hz**	**High Speed 480Hz**
TX channel #1 trip input	In #1	In #1	In #1	In #1	In #1	In #1
TX channel #2 trip input	In #2	In #2	In #2	In #2	In #2	In #2
TX channel #1 Guard	1680 Hz	1680 Hz	1680 Hzt	2040 Hz	2040 Hz	2040 Hz
TX channel #1 Trip	1440 Hz	1440 Hz	1440 Hz	1560 Hz	1560 Hz	1560 Hz
TX channel #2 Guard	1920 Hz	1920 Hz	1920 Hz	2520 Hz	2520 Hz	2520 Hz
TX channel #2 Trip	2160 Hz	2160 Hzt	2160 Hz	3000 Hz	3000 Hz	3000 Hz
RX channel #1 Guard	1680 Hz	1680 Hz	1680 Hz	2040 Hz	2040 Hz	2040 Hz
RX channel #1 Trip	1440 Hz	1440 Hz	1440 Hz	1560 Hz	1560 Hz	1560 Hz
RX channel #2 Guard	1920 Hz	1920 Hz	1920 Hz	2520 Hz	2520 Hz	2520 Hz
RX channel #2 Trip	2160 Hz	2160 Hz	2160 Hz	3000 Hz	3000 Hz	3000 Hz
RX thresholds (N / M)	6 / 8	4 / 8	3 / 8	6 / 8	4 / 8	3 / 8
RX channel #1, #2 qualifying time	10 mS	8 mS	5 mS	5 mS	4 mS	3 mS
RX channel #1, #2 inhibit onset	4 mS	3 mS	1 mS	4 mS	3 mS	2 mS
RX channel #1, #2 inhibit extend	50 mS	25 mS	10 mS	50 mS	25 mS	10 mS
RX channel #1, #2 detectors	BOTH	POLY	POLY	BOTH	POLY	POLY
RX channel #1, #2 averaging	ON	ON	OFF	ON	ON	OFF
RX channel #1 trip output	Out #1	Out #1	Out #1	Out #1	Out #1	Out #1
RX channel #2 trip output	Out #2	Out #2	Out #2	Out #2	Out #2	Out #2

NOTE: If two trip IO module are fitted, the VF defaults to two single channel commands. If one trip IO module is fitted, the VF defaults to one single channel command and the used TX/RX chanel is turned off.

VF Trip I/O Usage:- Common to all default VF settings	.
TRIP #1 (if not auto detected)	circuits 'ABC' on trip I/O module 1, no SIT
TRIP #2 (if not auto detected)	'Nil' circuits on trip I/O modules 2

VF Alarm relay allocation:- Common to all default VF settings.					
Alarm Source	Relay	Onset	Com'n Alarm	Latching	Relay State
VF TX FAIL	Relay # 1,	1 second	Include	Disabled	OFF
VF RX FAIL	Relay # 1,	1 second	Include	Disabled	OFF
VF INHIBIT FAIL	Relay # 1,	1 second	Include	Disabled	OFF
IDENT FAIL	Relay # 1,	1 second	Include	Disabled	OFF
TRIP 1,2 INPUT FAULT	Relay # 2,	1 second	Include	Disabled	OFF
TRIP 1,2 OUT FAULT	Relay # 2,	1 second	Include	Disabled	OFF
TRIP#1 REC'D Copy	Relay # 3,	0	Exclude	Disabled	ON
TRIP#2 REC'D Copy	Relay # 3,	0	Exclude	Disabled	ON
POWER SUPPLY WARNING	Relay # 4,	1 second	Include	Disabled	OFF
REMOTE TERM' FAIL	Relay # 5,	1 second	Include	Disabled	OFF
MONITOR FAULT	Relay # 6,	1 second	Include	Disabled	OFF
PROCESSOR FAULT	Relay # 6,	1 second	Include	Disabled	OFF
OFF NORMAL	Relay # 7,	1 second	Include	Disabled	OFF
TRIP#1 SENT Copy	Relay # 8,	0	Exclude	Disabled	ON
TRIP#2 SENT Copy	Relay # 8,	0	Exclude	Disabled	ON
TRIP 1,2 CUT-OFF	Relay # 10,	1 second	Include	Disabled	OFF
TRIP 1,2 HOLD-OFF	Relay # 10,	1 second	Include	Disabled	OFF
POWER FAIL	Not allocated,	0	Exclude	Disabled	NA
ACCESS	Not allocated,	1 second	Exclude	Disabled	NA
COMMON ALARM Copy	Not allocated,	1 second	Exclude	Disabled	NA

NOTE 1: Alarms with the ‘Copy’ suffix indicates alarms that are repeated from another event source (i.e. trip commands or the common alarm relay).
NOTE 2: Where the relay is not fitted, the relay allocation is changed to ‘Not allocated’.

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APPENDIX C

RS232, Modem and LAN Connections.

Information and setup menus can be accessed through the RS232 port, an external modem and to local terminals via the LAN. To connect the RS232 port to a personal computer (PC) or laptop, the DM1200 is connected to the PC's COM port. To access the DM1200 via a telephone line, an external modem is connected to the DM1200's RS232 port. The modem features in DM1200 are enabled in the setup menu. The modem functions in answer only mode.

RS232 connections to the DM1200 terminal are set to a default of 4800 baud, 8 data bits, no parity and 2 stop bits (4800 8N2)

DM1200 Terminal to Laptop or Personal Computer Cable Connections.

1200 9pin male	to	PC 9pin female	or	PC 25pin female
Pin 1	to	pin 1	or	pin 8,
Pin 2	to	pin 2	or	pin 3,
Pin 3	to	pin 3	or	pin 2,
Pin 4	to	pin 4	or	pin 20,
Pin 5	to	pin 5	or	pin 7,
Pin 6	to	pin 6	or	pin 6,
Pin 7	to	pin 7	or	pin 4,
Pin 8	to	pin 8	or	pin 5,
Pin 9	to	pin 9	or	pin 22.

NOTE 1: DM1200 terminal has 9 pin female 'D' type connector.
NOTE 2: On a PC fitted with a 9 pin male COM port connector, use a standard 9 pin extender cable.

DM1200 Terminal to External Modem Cable Connections.

1200 has female connector, Modem also has female connector.

1200 9pin DB male	to	Modem 9pin male	or	Modem 25pin male
Pin 1 DTR (out)	to	pin 4 DSR (in)	or	pin 20,
Pin 2 TX (out)	to	pin 3 RX (in)	or	pin 2,
Pin 3 RX (in)	to	pin 2 TX (out)	or	pin 3,
Pin 4 DSR (in)	to	pin 6 DTR (out)	or	pin 6,
Pin 5 Sig GND	to	pin 5 Sig GND	or	pin 7,
Pin 6 DTR (out)	to	N.C.		N.C.,
Pin 7 CTS (in)	to	pin 8 RTS (out)	or	pin 5,
Pin 8 RTS (out)	to	pin 7 CTS (in)	or	pin 4,
Pin 9 DTR (out)		N.C.		N.C.

DM1200 RS232 Terminal Program.

The DM1200TALK program is a video terminal emulation program designed to interface to the DM1200 terminal. The DM1200TALK program is run on the PC. Type *[F1]* for help screen.

DM1200TALK will work on an 4.77mHz XT as long as the COM port interrupts are functioning. It is not recommended running DM1200TALK through a COM port with no interrupt available.

VF Processor 1200-22 RS232 test and calibration cable connections,

1200-22 PL1 is male 0.1" 14way single in line connector on main PCB.

1200-22 PL1	to	PC 9pin female	or	PC 25pin female
N.C.		pin 1		pin 8,
Pin 2	to	pin 2	or	pin 3,
Pin 3	to	pin 3	or	pin 2,
N.C.		pin 4 link to 6		pin 20 link to 6,
Pin 1	to	pin 5	or	pin 7,
Pin 5	to	pin 7	or	pin 4,
Pin 4	to	pin 8	or	pin 5,
N.C.		pin 9	or	pin 22

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APPENDIX D

VF Processor Screens.

The VF Processor firmware contains data and status screens to facilitate calibration of the VF processor and aid in fault finding/repair.

These screens are accessed from the monitor through **MAINTENANCE**, **VIEW PROCESSOR** menu or by connecting PL1 (an RS232 port) on the VF processor to a PC / Laptop COM port. The DM1200TALK program is used on the PC / Laptop to communicate with the VF processor and display the data on the PC/Laptop's display.

Refer to Appendix C for the cable connections to the VF processor's RS232 port.

Many operations on the VF processor will stop normal trip processing. Selections that will cause this will generate a warning message on screen.

Main Screen

Example of screen;-

```
1200-22 V5.10 Diagnostic Menu. Checksum 0000.

SysTime=52224,VF Clock=1452Hz,Runtime 00:00:14.42,0016in/4912out,

 P=program EPLDS,    C=check EPLDS,        D=debug/faultfind,
 F=filter setup,     E=monitor data,       V=VF setup,
 Q=fast io state,    R=VF levels & alarms, J=Alarm Reasons,
 Z= setup & test,    M=channel spectrum analysis,
 Y=show calibration, T=check trip CCTs,    ESC=reset,
 S=save setup,

RAM 32767 has ERRORS / WARNINGS

OPERATION WARNING 10, Restart
```

The top line contains general information about version number, EPROM checksum, the number of recovered samples and the pointer in firmware execution where alarms or errors occurred.

The next line shows dynamic values of internal system time, VF sampling clock, runtime for reason code timing and the finally the number of correct data packets from / to the monitor module.

The next 6 lines are help lines indicating the key pressed to gain access to other screens and operations.

The last two lines shown are typical. The "errors / warnings" are expanded on subsequent lines to indicate the error or warning that has occurred. In this example the VF processor has been turned on.

Program EPLDs

Typing [P] in the main screen will cause the VF processor to verify the on-board EPLDs. If the EPLDs are not correct, the VF processor will erase, program and re-verify each EPLD in turn. If there is an EPLD failure, an error message will be displayed.

Check EPLDs

Typing [C] in the main screen will cause the VF processor to verify the on-board EPLDs. If the EPLDs do not verify an error message will be displayed.

Debug/Fault Find

Typing [D] in the main screen will cause the VF processor to display the debug/faultfind screen.

```
Debug, Waveform Generation and Fautlfinding Menu
IC12 Size=512, Data in IC12=512, Setup & Cal' in IC12=503
  [W] = write eeprom (IC12),  [R] = read eeprom (IC12),
  [E] = edit eeprom (IC12),   [V] = check ADC (IC14),
  [I] = input IO port,        [O] = output IO port,
  [P] = check DACs (IC31,IC30,IC19,IC34,IC24),
  [H] = calculator,
```

Typing the required letter allows various hardware functions to be stimulated. The calculator provides hexdecimal based number arithmetic to aid in checking hardware.

Filter Setup

Typing [F] in the main screen will cause the VF processor to display the filter setup screens. The user can toggle between filter groupings by typing numbers 1, 2, 3 or 4.

```
VF Filter Setup (errors are corrected), [N] next, [B] bandpass, [1,2,3,4].

RX1 MAX261s Mn, M, Fn,  F0out, F0calc,  Qn,  Qout, Qcalc, 1.63Gm, clk=384.0kHz
#1          2,  3, 36, 2444.6, 2465.7,  96,  2.00,  6.25
#2          2,  3, 13, 3174.8, 3259.7,  51,  0.83,  2.55
#3          2,  3, 27, 2686.4, 2761.0,  50,  0.82,  2.55
#4          2,  3,  4, 3595.0, 3650.1,  96,  2.00,  6.25

MF4-100 Filter clk=6857hz, LowPassWidth = 2932Hz to 3068Hz
```

Also provided is a filter shape table to check filter operation against calculated values. The screen can be toggled between full VF band and the VF channel. To leave the screen press escape.

```
RX1 VF band in use by MAX261s. [T] to toggle.
  300.0Hz      0.000out   -79.110dB
  485.0Hz      0.001out   -62.072dB
  670.0Hz      0.003out   -50.336dB
  855.0Hz      0.009out   -41.198dB
 1040.0Hz      0.021out   -33.574dB
 1225.0Hz      0.045out   -26.926dB
 1410.0Hz      0.090out   -20.954dB
 1595.0Hz      0.168out   -15.490dB
 1780.0Hz      0.300out   -10.460dB
 1965.0Hz      0.508out    -5.890dB
 2150.0Hz      0.800out    -1.940dB
 2335.0Hz      1.137out     1.112dB
 2520.0Hz      1.425out     3.076dB
 2705.0Hz      1.600out     4.082dB
 2890.0Hz      1.667out     4.438dB
 3075.0Hz      1.653out     4.365dB
 3260.0Hz      1.572out     3.931dB
 3445.0Hz      1.432out     3.121dB
 3630.0Hz      1.248out     1.921dB
 3815.0Hz      1.045out     0.380dB
 4000.0Hz      0.851out    -1.397dB
Bandpass Gain=  1.629, Q Gain=  1.000
```

Monitor Data

Typing [E] in the main screen will cause the VF processor to display the monitor data screen

```
V5.10  MONITOR Out Setup Data by value (RUN VF), [T] to toggle
NN=01, MM=02, Com Alarm=ON
Op MODE ->  Analogue (VF) Half Guard
Test Mode -> nil, Test Mask -> 00h
      Debounce, Input Extend, Output Extend
IO#1,    0.25mS,     0.10Sec,      0.10Sec
IO#2,    0.25mS,     0.10Sec,      0.10Sec
Hold Off=0.01Sec, Termination=0.00Sec

  V5.10  PROCESSOR Out Data by value (RUN VF)
Output Alarms; Short -> 07h, Opens IO#1 -> 00h, IO#2 -> 00h, Breakup -> 00h
Input Alarms; Open -> 0Fh, Short -> F0h, Breakup -> 00h
Alarms; VF -> 3008h Term'd -> 00h Hold Off -> 00h
Trip Received Reg -> 00h Trip Send Reg -> 00h G703 BER = 00000.
    Sent Count,  Received Count. Switch Open Alarms
IO#1        0        0           Tout-> 00h Gout-> 00h
IO#2        0        0           Tout-> 00h Gout-> 00h
Tx Send Pilot= 435.3mV, Rx Receive Pilot= 282.6mV
```

The user can toggle between a textual display and numeric display by typing [T].

```
MONITOR Setup and PROCESSOR Data in hex [T] toggle, [+] or [-]

       Data In ( NN )
Index       |   Data Out ( Output Switch Open Reg 1 )
    |       |          |
    0,   0001h,    0000h \
```

VF Setup

Typing [V] in the main screen will cause the VF processor to display the VF setup screen

```
VF Setup
    Trip (half) Guard (half) BandPass LEVdbm       Boost          IO
1   1440  1500  1680   1620  default    -5.0    -0.0 No Boost      1
2   2160  2100  1920   1980  default    -5.0    -0.0 No Boost      2

    Centre LPWidth BandPass MAXdbm  MINdbm  IO INHms QUALms CORms  EXTms
1   1560    240    default    +4.0   -15.0   1    5      4     5     50
2   2040    240    default    +4.0   -15.0   2    5      4     5     50

   Inhibit Operation       Discriminator Operation                    LoG Out#
1   Inh to Guard            Poly leads,Averaged  ,Wide LP,InhTrigAND, LoG Not Used
2   Inh to Guard            Poly leads,Averaged  ,Wide LP,InhTrigAND, LoG Not Used
```

Fast IO State

Typing [Q] in the main screen will cause the VF processor to display the trip IO status. Stimulating the trip IO cards will show the operation of the IO.

```
Trip IO State.

  FAST INPUT / OUTPUT REGISTERS.       Trip and Guard REGISTERS.
Inp1=00001000b   Out1=11110100b  Guard Send=11111111b  Guard Recd=11111111b
Inp2=00000111b   Out2=00000100b  Trip Send =00000000b  Trip Recd =00000000b

Send Count #1 =00000    Send Count #2 =00000          LoG Count #1 =00000
Recd Count #1 =00000    Recd Count #2 =00000          LoG Count #2 =00000

  TRIP INPUT Variables.
I#   Deb   Ext T-Deb T-Ext           Stage
1      0     0     0     0           Ready                 Hold Off= 000000
2      0     0     0     0            ????                 Cut Off = 000000

  TRIP OUTPUT Variables.
O#  ExtTimer CutTimer HoldTimer          Stage        LoG state
1          0         0         0          Ready        OFF
2          0         0         0           ????        OFF

                      Guard to Trip mS          Trip to Guard mS
O# HOLDOFF,CUTOFF  Min'  Last  Max'  Avg'    Min'  Last  Max'  Avg'
1  OFF     OFF     0.0   0.0   0.0   0.0     0.0   0.0   0.0   0.0   + GDelay
2  OFF     OFF     0.0   0.0   0.0   0.0     0.0   0.0   0.0   0.0   + GDelay
```

VF Levels and Alarms

Typing [R] in the main screen will cause the VF processor to display the VF level and alarm . Typing 0, 1, 2, 3, 4 or 5 will toggle between the screens for various sections.

Typing [0] shows line and alarm details.

```
VF Line Levels, [T]oggle, [0=line,1=Tx1,2=Tx2,3=Rx1,4=Rx2,5=DACs&Levels]
TX Line  ADC= 0528           Line low=OFF        Line high=OFF
         Lev=  435.3mV    -5.0dBm      (Lev max= 435.3mV)
         TX1=   -3.4dBm Low=OFF Hi=OFF
         TX2=   -0.3dBm Low=OFF Hi=ON


Rx line  DAC= 0041           Line Sig Lost=ON    Line Overload=OFF
         ADC= 0600 (ADCpeak=2773  LevPeak=  333.7mV  LoGupperADC=65535)
         Lev=    4.7mV   -43.0dBm       (Lev max=   4.7mV)
         RX1=  -43.0dBm Low=ON  Hi=OFF Lost=ON  Over=OFF Corr=OFF Inh=ON
         RX2=  -43.0dBm Low=ON  Hi=OFF Lost=ON  Over=OFF Corr=OFF Inh=ON
```

Typing [1] shows TX1details, typing [2] shows TX2.

```
VF LEVELS ch 1, [T]oggle, [0=line,1=Tx1,2=Tx2,3=Rx1,4=Rx2,5=DACs&Levels]
TX1 ON   DAC= 0516    Trip Bit=00000001b
         ADC= 0528
         BPgm= 1.54
         Lev=  520.8mV  (  -3.4dBm)
         Low=OFF
         Hi=OFF
```

Typing [3] shows RX1details, typing [4] shows RX2.

```
VF LEVELS ch 1 [T]oggle, [0=line,1=Tx1,2=Tx2,3=Rx1,4=Rx2,5=DACs&Levels]
                           RX1 ON    ADC= 1008           MDAC=0212
                                     Qgm=  1.00          BPgm= 1.63
                                     Lev=  161.5mV  ( -13.6dBm)


                                     SinAv=127 SinPk=021          Vmin=014
                                     CosAv=127 CosPk=035          Vmax=127
```

```
                                    Plo=OFF   Phi=ON    Pnoise=ON
         Trip Bit=00000001b
         Trip Msk=11111110b                           Psh90=010
        Guard Bit=00000000b                           Clip'g=OFF
        Guard Msk=11111111b         FastInh=ON        Zsiglost=OFF
                                    Zmin=014  Zcnt=010  Rthr=028  Zmax=032
                                    Zlo=OFF   Zhi=OFF   Znoise=ON
                                    InhNoiseTrigOred=OFF     LoGdet=OFF
                                    InhOnset=138      Correl'n=000
                                    TripQual=000      GurdQual=000

                                    PolyAvg=ON        PolyLed=ON
                                    Inh2Gud=ON        Hyster'=OFF
```

Typing [5] shows DAC and level details.

```
VF DACs and LEVELS, .[T]oggle, [0=line,1=Tx1,2=Tx2,3=Rx1,4=Rx2,5=DACs&Levels]
- Transmitters -                    - Receivers -

TX1 Set=    -5.0dBm                 Line DAC=  0041
TX1 DAC=  0520                      Lev(dBm)=   -43.0
TX1(dBm)=   -3.4
                                    Mod1 DAC=  4093
TX2 Set=    -5.0dBm                 RX1(dBm)=   -43.0
TX2 DAC=  0528
TX2(dBm)=   -0.3                    Mod2 DAC=  4093
                                    RX2(dBm)=   -43.0
Line(dBm)=  -5.0
```

Alarm Reasons

Typing [J] in the main screen will cause the VF processor to display the reasons for any previous alarm. Typing [C] will clear all reason codes. NOTE: that the lines can be wrapped on screen.

```
VF alarm reason codes, [C] to clear codes, [ESC] to leave.
VF#1 TX High:reason=,Line Lev,(Line Lev=0435mV,ADC=0528),(Channel Lev=0521mV,ADC
=0528), at 15:43:20.60
VF#1 RX Low:reason=,Channel Lev,(Line Lev=0005mV,DAC=0041,ADC=0600),(Channel Lev
=0005mV,DAC=4093,ADC=2064), at 16:07:49.05
VF#1 RX Inh:reason=,Channel Lev,Inhibit Timer,(Line Lev=0005mV,DAC=0041,ADC=0600
),(Channel Lev=0005mV,DAC=4093,ADC=2064), at 16:07:49.05
VF#1 RX Sig Lost:reason=,Channel Lev,(Line Lev=0005mV,DAC=0041,ADC=0600),(Channe
l Lev=0005mV,DAC=4093,ADC=2064), at 16:07:49.05
VF#1 RX Overload:reason=,Line Lev,(Line Lev=0005mV,DAC=0041,ADC=0600),(Channel L
ev=0005mV,DAC=4093,ADC=2064), at 16:07:49.10
VF#1 RX Discriminator:reason=,ZCross,Ratio,Detector Noise,FFT
VF#2 TX High:reason=,Channel Lev,(Line Lev=0435mV,ADC=0528),(Channel Lev=0744mV,
DAC=0528,ADC=0746), at 16:07:48.95
VF#2 RX Low:reason=,Channel Lev,(Line Lev=0005mV,DAC=0041,ADC=0600),(Channel Lev
=0005mV,DAC=4093,ADC=2064), at 16:07:48.35
VF#2 RX Inh:reason=,Channel Lev,Inhibit Timer,(Line Lev=0005mV,DAC=0041,ADC=0600
),(Channel Lev=0005mV,DAC=4093,ADC=2064), at 16:07:48.35
VF#2 RX Sig Lost:reason=,Channel Lev,(Line Lev=0005mV,DAC=0041,ADC=0600),(Channe
l Lev=0005mV,DAC=4093,ADC=2064), at 16:07:48.35
VF#2 RX Discriminator:reason=,ZCross,Ratio,Detector Noise,FFT
Alarm events TX=0, RX=0
RAM 32767 has ERRORS / WARNINGS
OPERATION WARNING 10, Restart
```

Setup & Test

Typing [Z] in the main screen will cause the VF processor to start the calibration functions. Typing [Esc] will abort calibration. If the VF processor finds errors or hardware problems during the calibration, an error message will be generated and the calibration will be aborted.

FFT Channel Spectrum Analysis

Typing [M] in the main screen will cause the VF processor to display the VF channel sprectum. Typing [T] will cause

the display to toggle between RX1 to RX2.

```
Spectrum ch#1, [T] to toggle.
0.017s  Sample
00064   Magnitude
+0032   Residual
00030   Op Hertz
ON      Inh' Flag
Amplitude, Hertz
  0         0.0
 19        30.2
  0        60.5
  6        90.8
  0       121.0
  4       151.2
  0       181.5
  3       211.8
```

Calibration Values

Typing [Y] in the main screen will cause the VF processor to display the processors calibration table. Typing [C] will cause the processor to re-check the calibration table showing errors on screen.

```
CALIBRATION VALUES. [C] to check tables. Other to leave.
             X1     Y1     X2     Y2     X3     Y3     X4     Y4 EPLD for
TX1 SetL   12.5   33.2   58.0  132.6  232.5  530.4  922.0 2121.6 MAX261
TX2 SetL   12.5   33.2   58.0  132.6  232.5  530.4  922.0 2121.6 MAX261
     TX1    8.5   12.5   56.8   58.0  274.5  232.5 1185.0  951.7 MAX261
     TX2    8.5   12.5   56.8   58.0  274.5  232.5 1185.0  951.7 MAX261
 TX Line   15.1   22.0  100.2   82.0  482.8  328.0 1979.0 1321.0 NA
 RX Line   39.6   22.0   99.6   82.0  379.3  328.0 1506.0 1321.0 NA
     RX1    0.8   12.5    2.9   58.0   11.6  232.5   46.1  922.0 MAX261
     RX2    0.8   12.5    2.9   58.0   11.6  232.5   46.1  922.0 MAX261
Using 8 FFT points for noise detection. Alarm Send Reset delay 20.
MF4 Filters are wide pass. Filters are error corrected.
Receiver line AGC is fast. Receiver modulator AGC is slow.
Cal Signature ->DM1200-22 V5.04 (Mon=V4.0B), Cal V5.04
Memory code = 0. (Zero Wait States) RAM <= 45nS, EPROM <= 45nS.
SetTX1    SetTX2    TX1       TX2       TX Line   RX Line   RX1       RX2
Ratio,Hz  Ratio,Hz  Ratio,Hz  Ratio,Hz  Ratio,Hz  Ratio,Hz  Ratio,Hz  Ratio,Hz
119/0420  119/0420  106/0420  106/0420  113/0420  113/0420  117/0420  117/0420
100/1800  100/1800  100/1800  100/1800  100/1800  100/1800  100/1800  100/1800
082/3825  082/3825  086/3825  086/3825  092/3825  086/3825  082/3825  082/3825
Frequency Factors -> TX line adc=1.00, RX line adc=1.00
TX1 1680hz setlev=0.98, adc=0.99, RX1 1680hz adc=0.99
TX2 1920hz setlev=1.01, adc=1.01, RX2 1920hz adc=1.01 -
```

Check Trip Circuits

Typing [T] in the main screen will cause the VF processor to display the trip IO self test results. Typing [Y] will cause the processor to perform a test procedure on the trip IO self test circuits.

```
OK to Check Trip IO auto test functions, [y] or [n] or [ESC] ?




OUTPUT O/C TRs,#1=No OPENS    ,#2=No OPENS

TRIP OUT S/C FAULTS ,CCT#1 = S/C ,CCT#2 = S/C ,CCT#3 = S/C

INPUT FAULTS ,T1=O/C ,G1=S/C          ,T2=O/C ,G2=S/C
```

Save Setup

Typing [S] in the main screen will cause the VF processor to resave the calibration in non-volatile EEPROM. This function is only for faultfinding the EEPROM and is not intended for calibration. After this operation the VF processor should be re-calibrated.

Reset

Typing [Esc] in the main screen will cause the VF processor to reset. This will cause all hardware and firmware to be re-initialised, as if power had been turned on.

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APPENDIX E

DM1200 System Ordering Part Numbers

DM1200**-P*-*T-R*	***Terminal model numbering***.	**Drawing No**	**Part Number**
	Relay Cards |		
	R1 = 1 card with 8 X 1c relays, 1200-12	P-313-114	00-0313-0114
	R2 = 2 cards with 8 x 1c relays, 1200-12	P-313-114	00-0313-0114
	TRIP I/O Module		
	1T = 1 module 340V 2.0A DC, 1200-32	P-313-313	00-0313-0313
	2T = 2 modules 340V 2.0A DC, 1200-32	P-313-313	00-0313-0313
	3T = 3 modules 340V 2.0A DC, 1200-32	P-313-313	00-0313-0313
	4T = 4 modules 340V 2.0A DC, 1200-32	P-313-313	00-0313-0313
	XX = No trip IO modules fitted.		
	Power Supply		
	P1 = 48 volt (20 to 60V DC), 1200-42	P-313-414	00-0313-0414
	P2 = 110 volt (90 to 320V), 1200-43	P-313-415	00-0313-0415
	Processor		
	A22 = VF Processor Module, 1200-22	P-313-203	00-0313-0203
	A23 = VF Processor Module, 1200-23	P-313-205	00-0313-0205
	D21 = G703 Processor Module, 1200-21	P-313-202	00-0313-0202
	D24 = G703 Processor Module, 1200-24	P-313-206	00-0313-0206
	D25 = RS422 Processor Module, 1200-25	P-313-207	00-0313-0207
	X = No processor fitted		
	Common Assembly		
	19" terminal. 1200-50	P-313-501	00-0313-0501
	Monitor Module, 1200-10B	P-313-106	00-0313-0106
EXTRAS-	***Extender Modules***		
	DM1200-X1 cabled for bench use, 1200-71	P-313-702	00-0313-0702
	DM1200-X2 one piece for rack use, 1200-70	P-313-701	00-0313-0701
	Manual for D21 and A22 processors		
	DM1200 Manual for D21 and A22 processors.	B-313-80/GP	00-0313-0080-GP
	Other Manuals for A23, D24 and D25 processors		
	DM1200 Installation and Operations Manual	B-313-88/OPS	00-0313-0088-1
	DM1200 Service Manual	B-313-88/TEC	00-0313-0088-2
	DM1200 Installation, Operations and Service Manual (in 1 binder)	B-313-88/FUL	00-0313-0088-3
	DM1200 Full Manual on CD, PC (or Laptop) setup.exe installation file.	B-313-88/CD	00-0313-0088-CD